Si9945BDY

RoHS

COMPLIANT

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Vishay Siliconix

Dual N-Channel 60 V (D-S) MOSFET



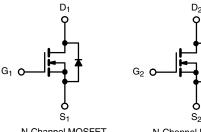
PRODUCT SUMMARY					
V _{DS} (V)	60				
$R_{DS(on)}$ max. (Ω) at V_GS = 10 V	0.058				
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.072				
Q _g typ. (nC)	13				
I _D (A) ^a	5.3				
Configuration	Dual				

FEATURES

- TrenchFET[®] power MOSFET
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- LCD TV CCFL inverter
- · Load switch



N-Channel MOSFET

S2 N-Channel MOSFET

ORDERING INFORMATION				
Package	SO-8			
Lead (Pb)-free and halogen-free	Si9945BDY-T1-GE3			

ABSOLUTE MAXIMUM RATINGS	$(T_A = 25 \ ^\circ C, unless)$	s otherwise note	d)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	60	V	
Gate-source voltage		V _{GS}	± 20	v	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		5.3		
	T _C = 70 °C		4.3		
	T _A = 25 °C	I _D	4.3 ^{b, c}		
	T _A = 70 °C		3.4 ^{b, c}	•	
Pulsed drain current (10 µs width)		I _{DM}	20	— A	
Continuous source-drain diode current	T _C = 25 °C		2.6		
	T _A = 25 °C	I _S	1.7 ^{b, c}		
Avalanche current	L = 0 1 mH	I _{AS}	11		
Single-pulse avalanche energy		E _{AS}	6.1	mJ	
Maximum power dissipation	T _C = 25 °C		3.1		
	T _C = 70 °C		2	w	
	T _A = 25 °C	P _D	2 ^{b, c}	vv	
	T _A = 70 °C	1	1.3 ^{b, c}		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^{a, d}		R _{thJA}	55	62.5	°C/W	
Maximum junction-to-foot (drain)	Steady state	R _{thJF}	33	40	C/W	

Notes

a. Based on $T_C = 25 \ ^{\circ}C$

b. Surface mounted on 1" x 1" FR4 board

t = 10 s c.

d. Maximum under steady state conditions is 110 °C/W

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static	<u> </u>						
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	60	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	L 050 A	-	55	-	mV/°C	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-6	-		
		$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1	-	3	v	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 5 \text{ mA}$	-	2.5	-		
Gate-source leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = 20 V$	-	-	100	nA	
Zara gata valtaga drain aurrant		$V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1	1 10 μΑ	
Zero gate voltage drain current	IDSS	$V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 85 ^{\circ}\text{C}$	-	-	10		
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20	-	-	Α	
	D	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 4.3 \text{ A}$	-	0.046	0.058	Ω	
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 3.9 \text{ A}$	-	0.059	0.072		
Forward transconductance ^a	g _{fs}	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 4.3 \text{ A}$	-	15	-	S	
Dynamic ^b							
Input capacitance	C _{iss}		-	665	-	pF	
Output capacitance	Coss	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	75	-		
Reverse transfer capacitance	C _{rss}		-	40	-		
-		$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4.3 \text{ A}$	-	13	20	-	
Total gate charge	Qg		-	6	9	nC	
Gate-source charge	Q _{gs}	V_{DS} = 30 V, V_{GS} = 4.5 V, I_D = 4.3 A	-	2.3	-		
Gate-drain charge	Q _{gd}		-	2.6	-		
Gate resistance	Rg	f = 1 MHz	-	2	-	Ω	
Turn-on delay time	t _{d(on)}		-	15	25		
Rise time	tr	$V_{DD} = 30 \text{ V}, \text{ R}_{\text{I}} = 8.8 \Omega,$	-	65	100		
Turn-off delay time	t _{d(off)}	$I_D \cong 3.4$ Å, $V_{GEN} = 4.5$ V, $R_g = 1$ Ω	-	15	25		
Fall time	t _f		-	10	15		
Turn-on delay time	t _{d(on)}		-	10	15	ns	
Rise time	tr	$V_{DD} = 30 \text{ V}, \text{ R}_{L} = 8.8 \Omega,$	-	15	25	1	
Turn-off delay time	t _{d(off)}	$I_D \cong 3.4 \text{ A}, V_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega$	-	20	30	-	
Fall time	t _f		-	10	15	1	
Drain-Source Body Diode Characteris	tics			•			
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	2.6		
Pulse diode forward current	I _{SM}	-	-	-	20	A	
Body diode voltage	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	-	0.8	1.2	V	
Body diode reverse recovery time	t _{rr}		-	30	60	ns	
Body diode reverse recovery charge	Q _{rr}	I _F = 1.7 A, di/dt = 100 A/μs,	-	32	50	nC	
Reverse recovery fall time	ta	$T_{\rm J} = 25 \ ^{\circ}{\rm C}$	-	25	-	1	
Reverse recovery rise time	t _b		-	5	-	ns	

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

b. Guaranteed by design, not subject to production testing

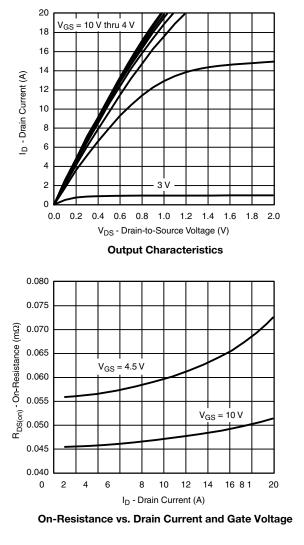
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

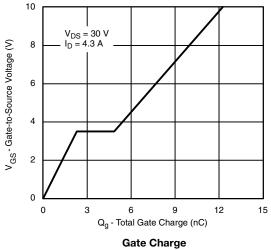
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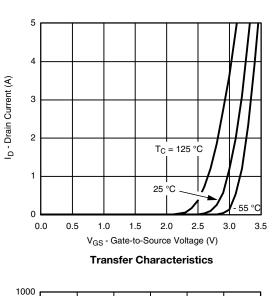


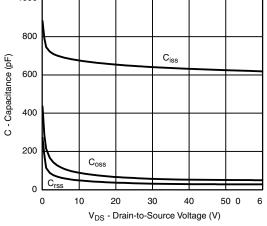
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

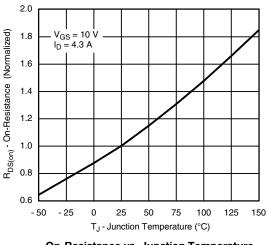








Capacitance



On-Resistance vs. Junction Temperature

S09-0321-Rev. A, 02-Mar-09

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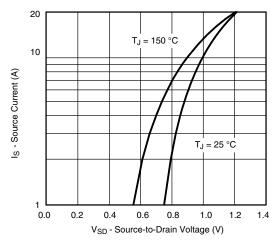
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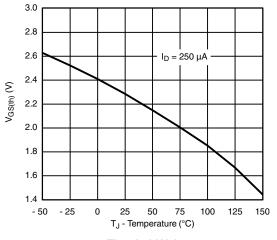
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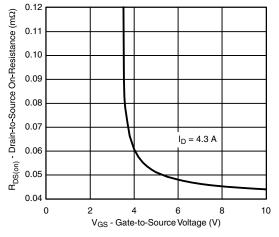
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



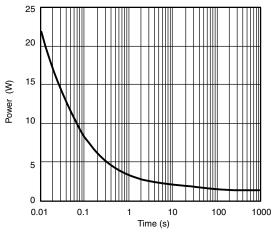
Source-Drain Diode Forward Voltage



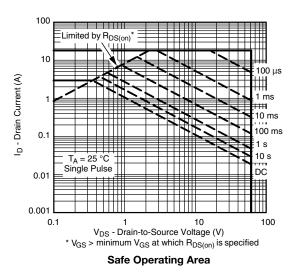




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



4

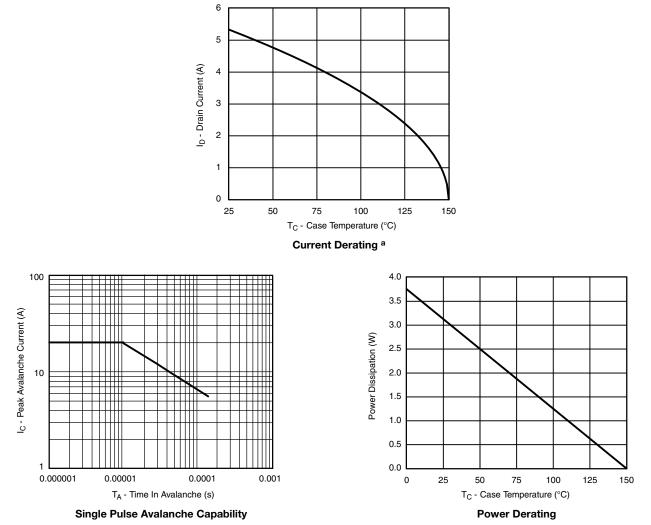
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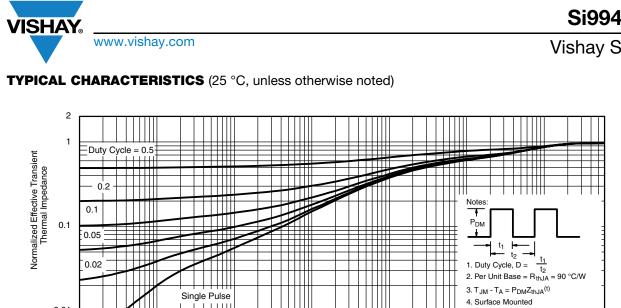
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



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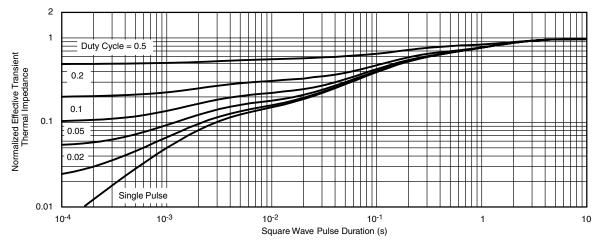


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100

600



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?64737.

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Package Information

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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





	MILLIMETERS		INC	HES	
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					

Application Note 826

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RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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