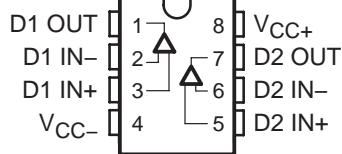


# THS6052, THS6053 175 mA, $\pm 12$ V ADSL CPE LINE DRIVERS

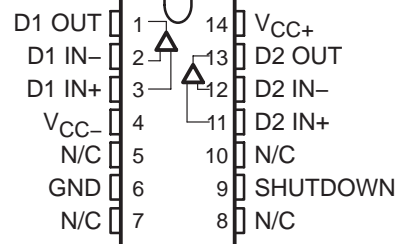
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- **Remote Terminal ADSL Line Driver**
  - Ideal for Both Full Rate ADSL and G.Lite
  - Compatible With 1:1 Transformer Ratio
- **Low 2.7 pA/ $\sqrt{\text{Hz}}$  Noninverting Current Noise**
  - Reduces Noise Feedback Through Hybrid Into Downstream Channel
- **Wide Supply Voltage Range  $\pm 5$  V to  $\pm 15$  V**
  - Ideal for  $\pm 12$ -V Operation
- **Wide Output Swing**
  - 42 Vpp Differential Output Voltage,  $R_L = 200 \Omega$ ,  $\pm 12$ -V Supply
- **High Output Current**
  - 175 mA (typ)
- **High Speed**
  - 110 MHz ( $-3$  dB,  $G=8$ ,  $\pm 12$  V)
  - 1500 V/ $\mu\text{s}$  Slew Rate ( $G = 8$ ,  $\pm 12$  V)
- **Low Distortion, Single-Ended,  $G = 8$** 
  - $-83$  dBc (250 kHz, 2 Vpp, 100- $\Omega$  load)
- **Low Power Shutdown (THS6053)**
  - 300- $\mu\text{A}$  Total Standby Current
- **Thermal Shutdown and Short Circuit Protection**
- **Standard SOIC, SOIC PowerPAD, and TSSOP PowerPAD™ Package**
- **Evaluation Module Available**

THS6052  
SOIC (D) AND  
SOIC PowerPAD™ (DDA) PACKAGE  
(TOP VIEW)

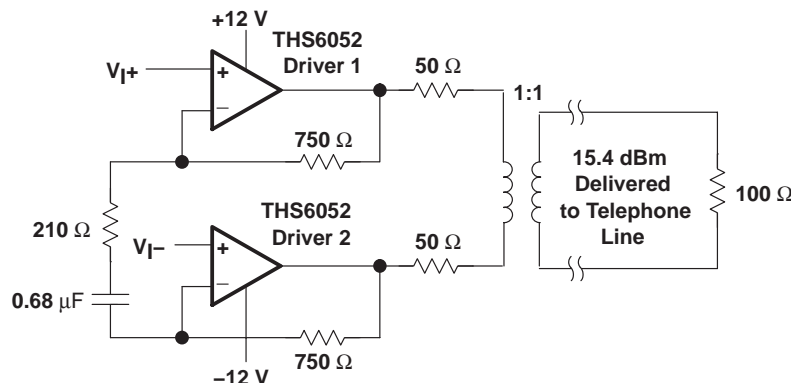


THS6053  
SOIC (D) AND  
TSSOP PowerPAD™ (PWP) PACKAGE  
(TOP VIEW)



## description

The THS6052/3 is a high-speed line driver ideal for driving signals from the remote terminal to the central office in asymmetrical digital subscriber line (ADSL) applications. It can operate from  $\pm 12$ -V supply voltages while drawing only 5.2 mA of supply current per channel. It offers low  $-83$  dBc total harmonic distortion driving a 100- $\Omega$  load (2 Vpp). The THS6052/3 offers a high 42-Vpp differential output swing across a 200- $\Omega$  load from a  $\pm 12$ -V supply. The THS6053 features a low-power shutdown mode, consuming only 300  $\mu\text{A}$  quiescent current per channel. The THS6052/3 is packaged in a standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD™ packages.



## RELATED PRODUCTS

DEVICE	DESCRIPTION
THS6042/3	350-mA, $\pm 12$ V ADSL CPE line driver
THS6092/3	275-mA, +12 V ADSL CPE line driver
OPA2677	380-mA, +12 V ADSL CPE line driver
THS6062	Low noise ADSL receiver



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# THS6052, THS6053 175 mA, ±12 V ADSL CPE LINE DRIVERS

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## AVAILABLE OPTION

T <sub>A</sub>	PACKAGED DEVICE				EVALUATION MODULES
	SOIC-8 (D)	SOIC-8 PowerPAD (DDA)	SOIC-14 (D)	TSSOP-14 (PWP)	
0°C to 70°C	THS6052CD	THS6052CDDA	THS6053CD	THS6053CPWP	THS6052EVM THS6053EVM
-40°C to 85°C	THS6052ID	THS6052IDDA	THS6053ID	THS6053IPWP	—

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V <sub>CC+</sub> to V <sub>CC-</sub>	33 V
Input voltage	± V <sub>CC</sub>
Output current (see Note 1)	275 mA
Differential input voltage	± 4 V
Maximum junction temperature	150°C
Total power dissipation at (or below) 25°C free-air temperature	See Dissipation Ratings Table
Operating free-air temperature, T <sub>A</sub> : Commercial	0°C to 70°C
Industrial	-40°C to 85°C
Storage temperature, T <sub>stg</sub> : Commercial	-65°C to 125°C
Industrial	-65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS6052 and THS6053 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 for more information about utilizing the PowerPAD™ thermally enhanced package.

## DISSIPATION RATING TABLE

PACKAGE	θ <sub>JA</sub>	θ <sub>JC</sub>	T <sub>A</sub> = 25°C T <sub>J</sub> = 150°C POWER RATING
D-8	95°C/W‡	38.3°C/W‡	1.32 W
DDA	45.8°C/W‡	9.2°C/W‡	2.73 W
D-14	66.6°C/W‡	26.9°C/W‡	1.88 W
PWP	37.5°C/W	1.4°C/W	3.3 W

‡ This data was taken using the JEDEC proposed high-K test PCB. For the JEDEC low-K test PCB, the θ<sub>JA</sub> is 168°C/W for the D-8 package and 122.3°C/W for the D-14 package.

## recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC+</sub> to V <sub>CC-</sub>	Dual supply	±5		±15	V
	Single supply	10		30	
Operating free-air temperature, T <sub>A</sub>	C-suffix	0		70	°C
	I-suffix	-40		85	



electrical characteristics over recommended operating free-air temperature range,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = \pm 12\text{ V}$ ,  $R_{FEEDBACK} = 750\ \Omega$ ,  $R_L = 100\ \Omega$  (unless otherwise noted)

**dynamic performance**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BW	Small-signal bandwidth (–3 dB)	$R_L = 50\ \Omega$	G= 1, $R_F = 1\ \text{k}\Omega$	$V_{CC} = \pm 5\ \text{V}$	110		MHz
				$V_{CC} = \pm 12\ \text{V}$	120		
			G= 2, $R_F = 680\ \Omega$	100			
				G= 8, $R_F = 330\ \Omega$	$V_{CC} = \pm 5\ \text{V}, \pm 12\ \text{V}$		
		$R_L = 100\ \Omega$	G= 1, $R_F = 1\ \text{k}\Omega$		$V_{CC} = \pm 5\ \text{V}$	150	
				$V_{CC} = \pm 12\ \text{V}$	170		
			G= 2, $R_F = 680\ \Omega$	135			
				G= 8, $R_F = 330\ \Omega$	$V_{CC} = \pm 5\ \text{V}, \pm 12\ \text{V}$		
SR	Slew rate (see Note 2), G=8	$V_O = 4\ V_{PP}$	$V_{CC} = \pm 5\ \text{V}$		$V_{CC} = \pm 5\ \text{V}$	650	
			$V_{CC} = \pm 12\ \text{V}$	$V_{CC} = \pm 12\ \text{V}$	850		
			$V_{CC} = \pm 15\ \text{V}$	$V_{CC} = \pm 15\ \text{V}$	950		
		$V_O = 16\ V_{PP}$	$V_{CC} = \pm 12\ \text{V}$	$V_{CC} = \pm 12\ \text{V}$	1500		
			$V_{CC} = \pm 15\ \text{V}$	$V_{CC} = \pm 15\ \text{V}$	1700		
				$V_{CC} = \pm 15\ \text{V}$	$V_{CC} = \pm 15\ \text{V}$	1700	

NOTE 2: Slew rate is defined from the 25% to the 75% output levels.

**noise/distortion performance**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion (single-ended configuration)	Gain = 8, $R_L = 100\ \Omega$ , $V_{CC} = \pm 12\ \text{V}$ , $f = 250\ \text{kHz}$	$V_O(pp) = 2\ \text{V}$	–83		dBc	
			$V_O(pp) = 16\ \text{V}$	–78			
		Gain = 8, $R_L = 50\ \Omega$ , $V_{CC} = \pm 5\ \text{V}$ , $f = 250\ \text{kHz}$	$V_O(pp) = 2\ \text{V}$	–74			
			$V_O(pp) = 6\ \text{V}$	–72			
$V_n$	Input voltage noise	$V_{CC} = \pm 5\ \text{V}$ , $f = 10\ \text{kHz}$ , $\pm 12\ \text{V}$		2.1		nV/ $\sqrt{\text{Hz}}$	
$I_n$	Input current noise	+Input	$f = 10\ \text{kHz}$ , $V_{CC} = \pm 5\ \text{V}$ , $V_{CC} = \pm 12\ \text{V}$ , $V_{CC} = \pm 15\ \text{V}$	2.7		pA/ $\sqrt{\text{Hz}}$	
		–Input		10.7			
$X_T$	Crosstalk	$f = 250\ \text{kHz}$ , G = 2, $R_L = 100\ \Omega$	$V_{CC} = \pm 12\ \text{V}$ , $R_L = 100\ \Omega$	$V_O = 2\ \text{Vp-p}$	–79		dBc
		$f = 250\ \text{kHz}$ , G = 2, $R_L = 50\ \Omega$	$V_{CC} = \pm 5\ \text{V}$ , $R_L = 50\ \Omega$	$V_O = 2\ \text{Vp-p}$	–71		

# THS6052, THS6053

## 175 mA, $\pm 12$ V ADSL CPE LINE DRIVERS

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electrical characteristics over recommended operating free-air temperature range,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = \pm 12$  V,  $R_{FEEDBACK} = 750\ \Omega$ ,  $R_L = 100\ \Omega$  (unless otherwise noted) (continued)

### dc performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OS</sub>	Input offset voltage	$V_{CC} = \pm 12$ V, $V_{CC} = \pm 6$ V	$T_A = 25^\circ\text{C}$	5	10	mV
			$T_A = \text{full range}$		15	
	Differential offset voltage		$T_A = 25^\circ\text{C}$	3	6	
			$T_A = \text{full range}$		8	
Offset drift		$T_A = \text{full range}$		30	$\mu\text{V}/^\circ\text{C}$	
I <sub>IB</sub>	– Input bias current	$V_{CC} = \pm 12$ V, $V_{CC} = \pm 6$ V	$T_A = 25^\circ\text{C}$	5	10	$\mu\text{A}$
			$T_A = \text{full range}$		12	
	+ Input bias current		$T_A = 25^\circ\text{C}$	2	5	
			$T_A = \text{full range}$		6	
	Differential input bias current		$T_A = 25^\circ\text{C}$	5	10	
$T_A = \text{full range}$			12			
Z <sub>OL</sub>	Open loop transimpedance	$V_{CC} = \pm 12$ V, $V_{CC} = \pm 6$ V	$R_L = 1\ \text{k}\Omega$ ,	1		M $\Omega$

### input characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>ICR</sub>	Input common-mode voltage range	$V_{CC} = \pm 12$ V	$\pm 9.7$	$\pm 10.1$		V
		$V_{CC} = \pm 6$ V	$\pm 3.8$	$\pm 4.2$		
CMRR	Common-mode rejection ratio	$V_{CC} = \pm 12$ V, $V_{CC} = \pm 6$ V	$T_A = 25^\circ\text{C}$	59	66	dB
			$T_A = \text{full range}$	57		
R <sub>I</sub>	Input resistance	+ Input		1.5		M $\Omega$
		– Input		15		$\Omega$
C <sub>I</sub>	Input capacitance			2		pF

### output characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>O</sub>	Output voltage swing	$R_L = 50\ \Omega$ , $V_{CC} = \pm 6$ V		$\pm 4.2$	$\pm 4.6$	V
			Single ended			
		$R_L = 100\ \Omega$	$V_{CC} = \pm 12$ V	$\pm 10.1$	$\pm 10.5$	
		$V_{CC} = \pm 6$ V	$\pm 4.4$	$\pm 4.8$		
I <sub>O</sub>	Output current	$R_L = 25\ \Omega$ , $V_{CC} = \pm 12$ V	150	175	mA	
		$R_L = 10\ \Omega$ , $V_{CC} = \pm 6$ V	150	175		
I <sub>SC</sub>	Short-circuit current	$R_L = 0\ \Omega$ , $V_{CC} = \pm 12$ V		250		mA
	Output resistance	Open loop		14		$\Omega$



# THS6052, THS6053

## 175 mA, $\pm 12$ V ADSL CPE LINE DRIVERS

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electrical characteristics over recommended operating free-air temperature range,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = \pm 12$  V,  $R_{FEEDBACK} = 750 \Omega$ ,  $R_L = 100 \Omega$  (unless otherwise noted) (continued)

### power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{CC}$	Operating range	Dual supply		$\pm 4.5$		$\pm 16.5$	V
		Single supply		9		33	
$I_{CC}$	Quiescent current (each driver)	$V_{CC} = \pm 12$ V	$T_A = 25^\circ\text{C}$		5.2	7	mA
			$T_A = \text{full range}$			8	
		$V_{CC} = \pm 6$ V	$T_A = 25^\circ\text{C}$		4.5	6.5	
			$T_A = \text{full range}$			7.5	
PSRR	Power supply rejection ratio	$V_{CC} = \pm 12$ V	$T_A = 25^\circ\text{C}$	-64	-62		dB
			$T_A = \text{full range}$		-61	-	
		$V_{CC} = \pm 6$ V	$T_A = 25^\circ\text{C}$		-60	-70	
			$T_A = \text{full range}$			-58	

### shutdown characteristics (THS6053 only)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IL}(\text{SHDN})$	Shutdown pin voltage for power up	$V_{CC} = \pm 6$ V, $\pm 12$ V GND = 0 V, (GND Pin as Reference)				0.8	V
$V_{IH}(\text{SHDN})$	Shutdown pin voltage for power down	$V_{CC} = \pm 6$ V, $\pm 12$ V, GND = 0 V, (GND Pin as Reference)		2			V
$I_{CC}(\text{SHDN})$	Total quiescent current when in shutdown state	$V_{GND} = 0$ V, $V_{CC} = \pm 6$ V, $\pm 12$ V			0.3	0.7	mA
$t_{DIS}$	Disable time (see Note 3)	$V_{CC} = \pm 12$ V			0.1		$\mu\text{s}$
$t_{EN}$	Enable time (see Note 3)	$V_{CC} = \pm 12$ V			0.4		$\mu\text{s}$
$I_{IL}(\text{SHDN})$	Shutdown pin input bias current for power up	$V_{CC} = \pm 6$ V, $\pm 12$ V			40	100	$\mu\text{A}$
$I_{IH}(\text{SHDN})$	Shutdown pin input bias current for power down	$V_{CC} = \pm 6$ V, $\pm 12$ V, $V(\text{SHDN}) = 3.3$ V			50	100	$\mu\text{A}$

NOTE 3: Disable/enable time is defined as the time from when the shutdown signal is applied to the SHDN pin to when the supply current has reached half of its final value.

# THS6052, THS6053 175 mA, $\pm 12$ V ADSL CPE LINE DRIVERS

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## APPLICATION INFORMATION

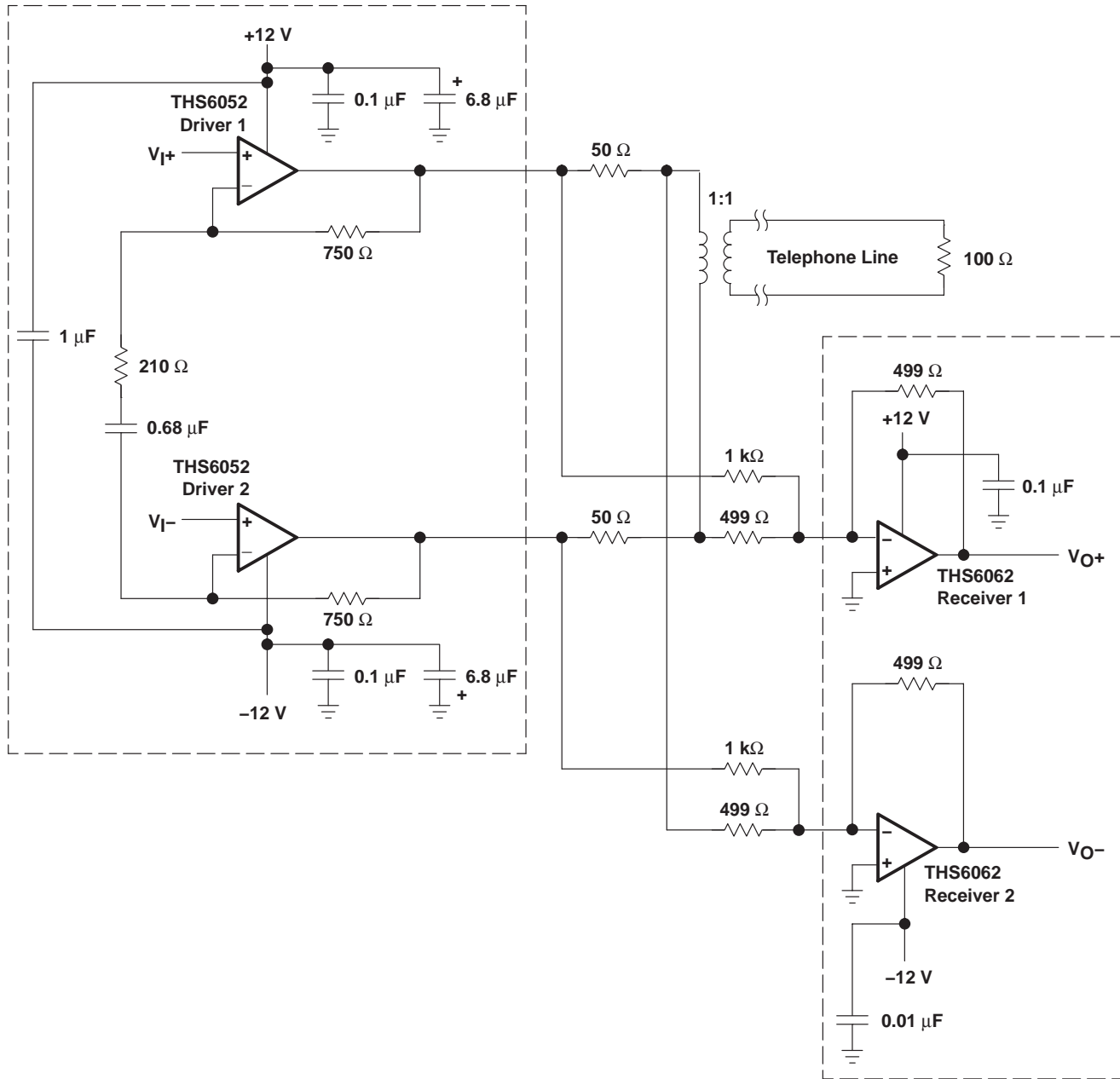


Figure 1. THS6052 ADSL Application With 1:1 Transformer Ratio

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS6052CDDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	6052C	<a href="#">Samples</a>
THS6052ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6052I	<a href="#">Samples</a>
THS6052IDDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	6052I	<a href="#">Samples</a>
THS6053CPWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HS6053C	<a href="#">Samples</a>
THS6053IPWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS6053I	<a href="#">Samples</a>
THS6053IPWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS6053I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

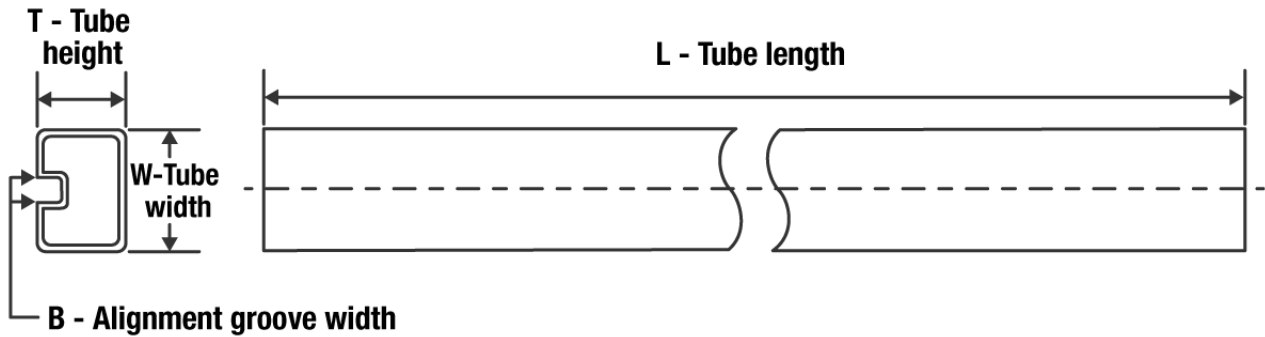

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6053CPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
THS6053IPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6053CPWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0
THS6053IPWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0

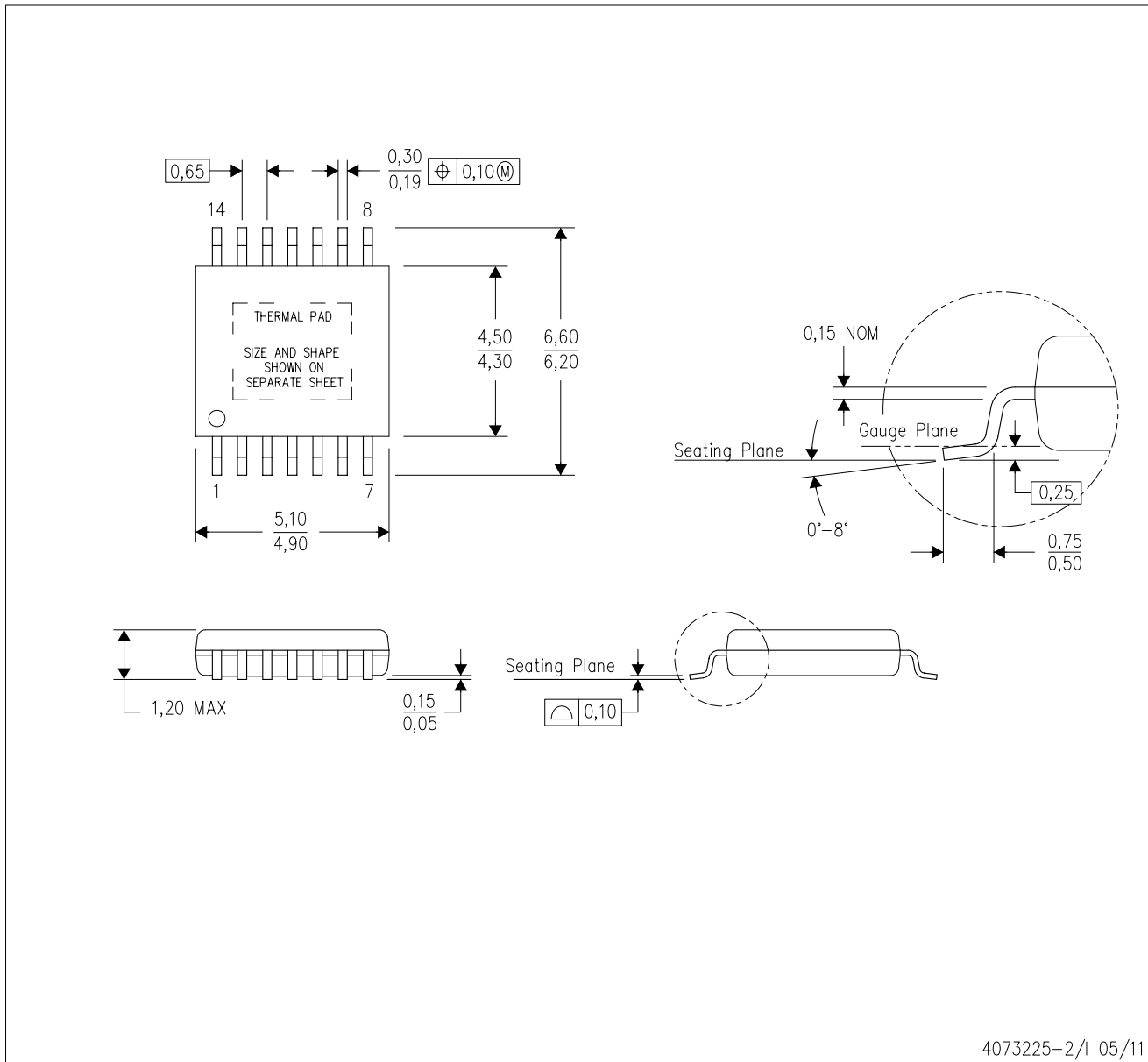
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
THS6052CDDA	DDA	HSOIC	8	75	505.46	6.76	3810	4
THS6052ID	D	SOIC	8	75	505.46	6.76	3810	4
THS6052IDDA	DDA	HSOIC	8	75	505.46	6.76	3810	4
THS6053IPWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5

PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-2/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

## THERMAL PAD MECHANICAL DATA

PWP (R-PDSO-G14)

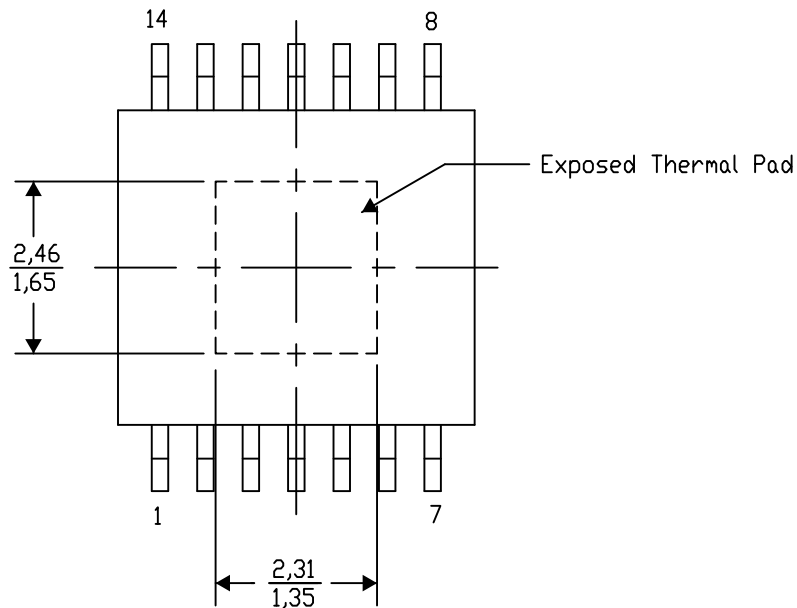
PowerPAD™ SMALL PLASTIC OUTLINE

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# THERMAL PAD MECHANICAL DATA

PWP (R-PDSO-G14)

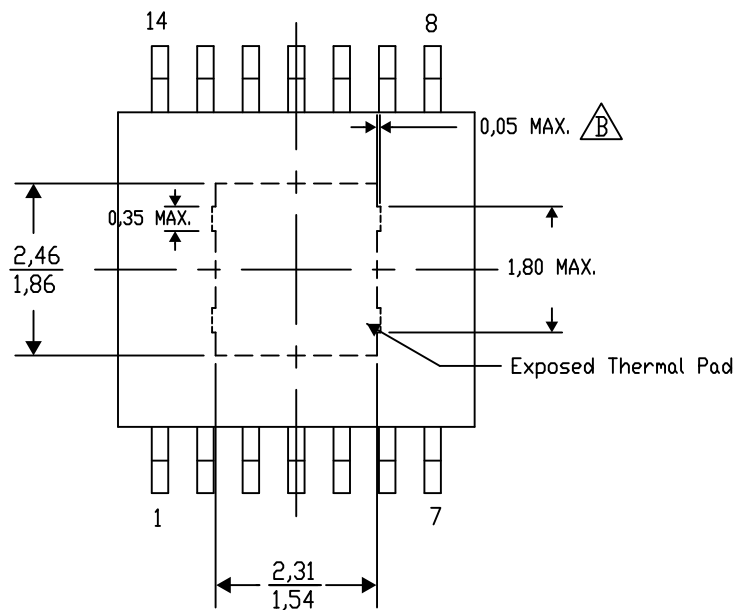
PowerPAD™ SMALL PLASTIC OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

4206332-44/AO 01/16

NOTE: A. All linear dimensions are in millimeters

 Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



4207609-2/W 09/15

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

# DDA0008B



# PACKAGE OUTLINE

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



### NOTES:

PowerPAD is a trademark of Texas Instruments.

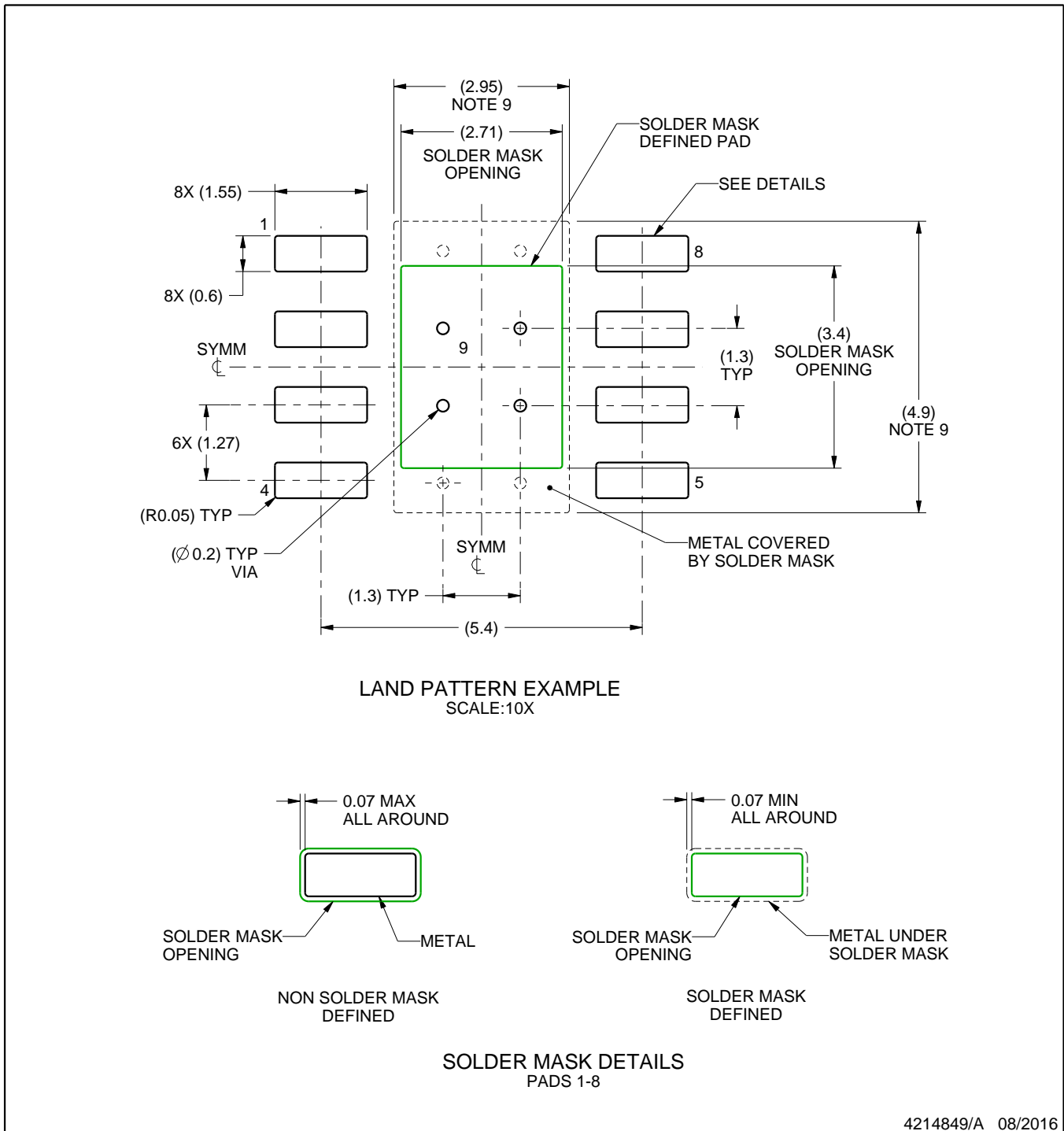
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

# EXAMPLE BOARD LAYOUT

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4214849/A 08/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
 EXPOSED PAD  
 100% PRINTED SOLDER COVERAGE BY AREA  
 SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

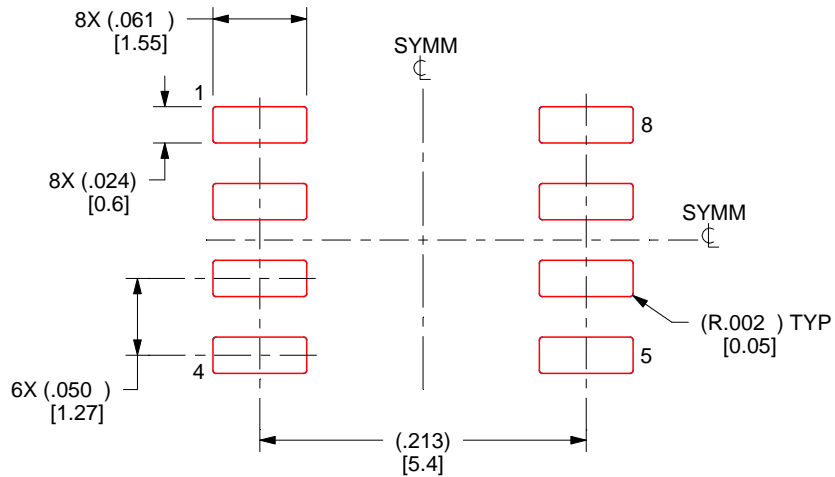
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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