



PMDPB58UPE

20 V dual P-channel Trench MOSFET

3 February 2016

Product data sheet

1. General description

Dual small-signal P-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- 2 kV ElectroStatic Discharge (ESD) protection

3. Applications

- Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

4. Quick reference data

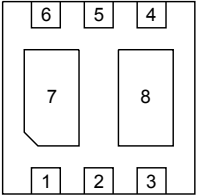
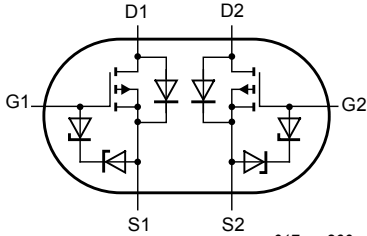
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-20	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}$; $T_{amb} = 25\text{ °C}$; $t \leq 5\text{ s}$	[1]	-	-4.5	A
Static characteristics (per transistor)						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}$; $I_D = -2\text{ A}$; $T_j = 25\text{ °C}$	-	58	67	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 Transparent top view DFN2020-6 (SOT1118)	 017aaa260
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMDPB58UPE	DFN2020-6	DFN2020-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118

7. Marking

Table 4. Marking codes

Type number	Marking code
PMDPB58UPE	2A

8. Limiting values

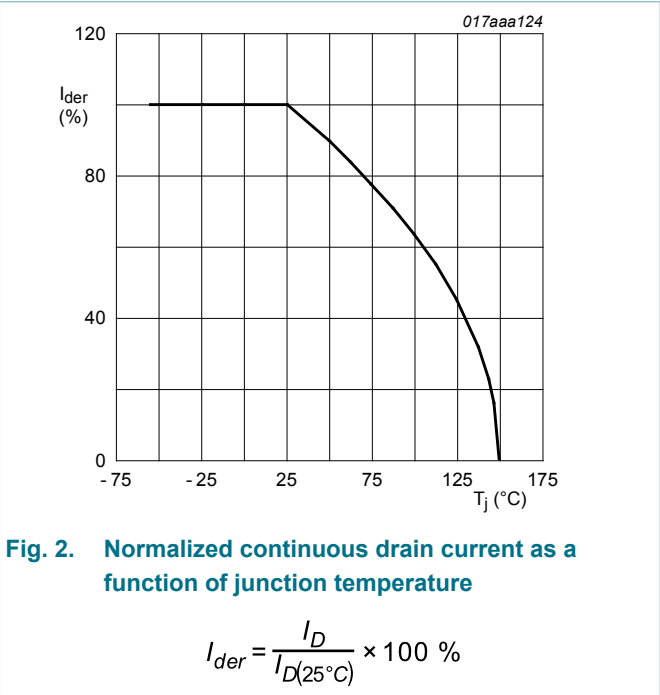
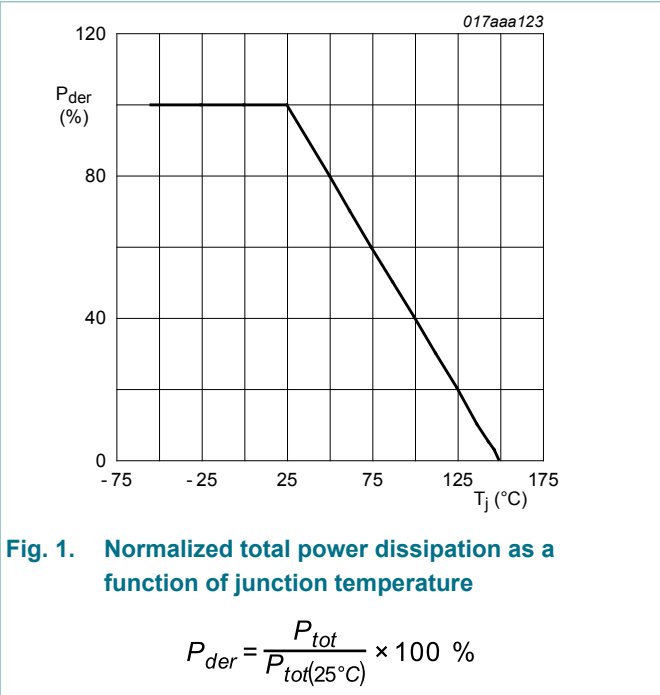
Table 5. Limiting values

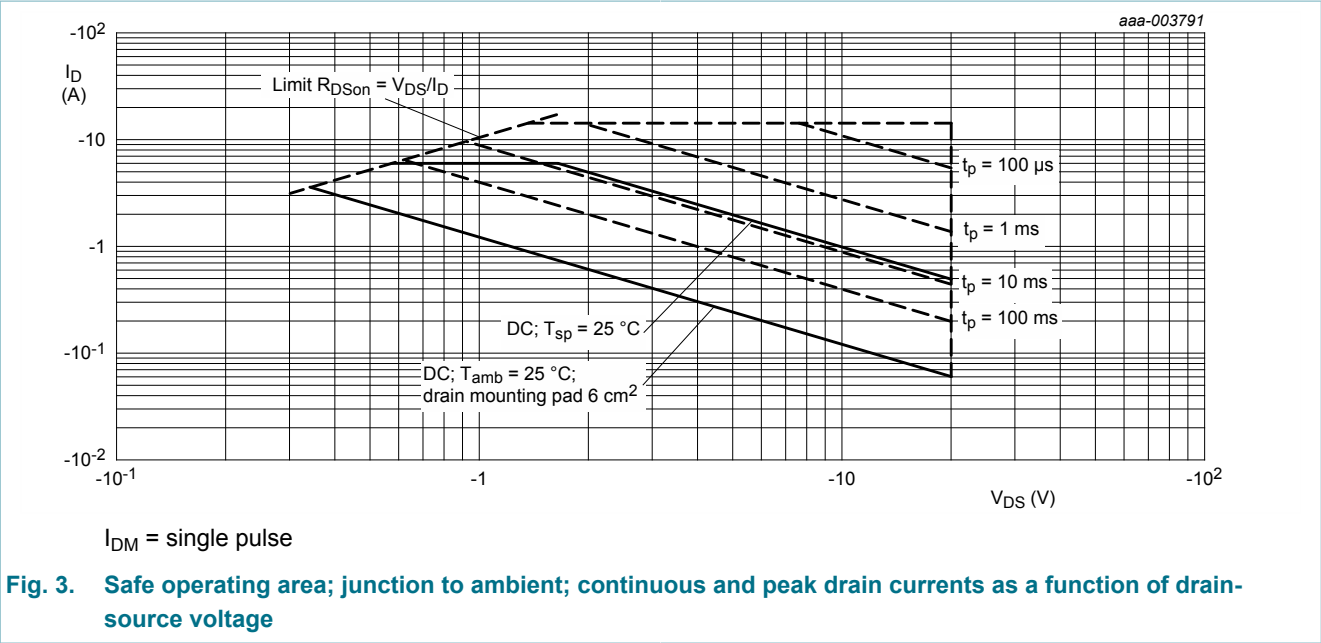
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	-20	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}; t \leq 5\text{ s}$	[1]	-	-4.5	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-3.6	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ }^{\circ}\text{C}$	[1]	-	-2.3	A

Symbol	Parameter	Conditions		Min	Max	Unit
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-14.4	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	515	mW
			[1]	-	1210	mW
		T _{sp} = 25 °C		-	8330	mW
Per device						
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-1.3	A
ESD maximum rating						
V _{ESD}	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 kΩ	[3]	-	2000	V

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	212	244	K/W
			[2]	-	90	104	K/W
		in free air; t ≤ 5 s	[2]	-	55	64	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	11	15	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

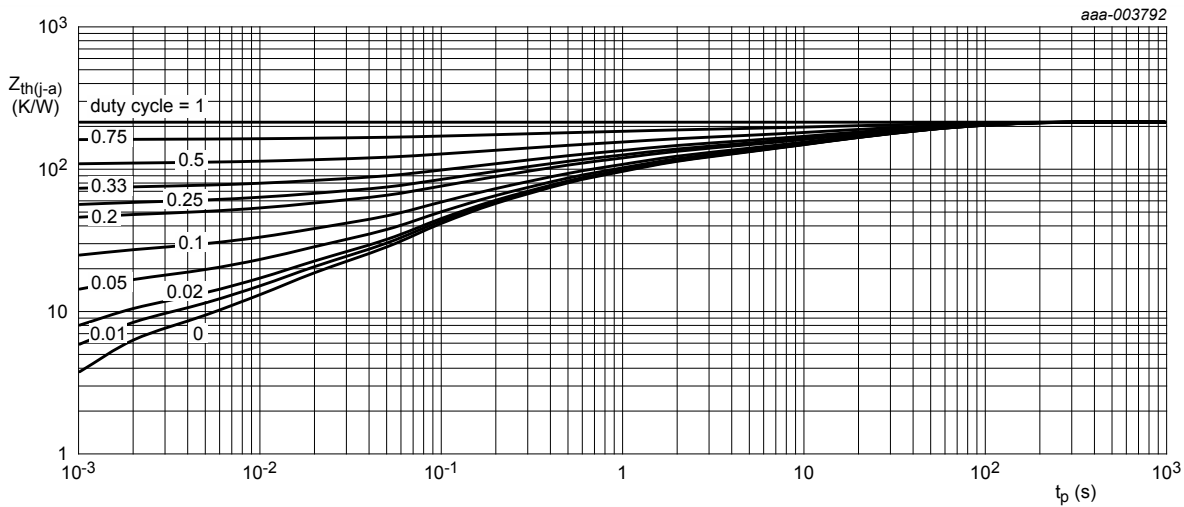


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

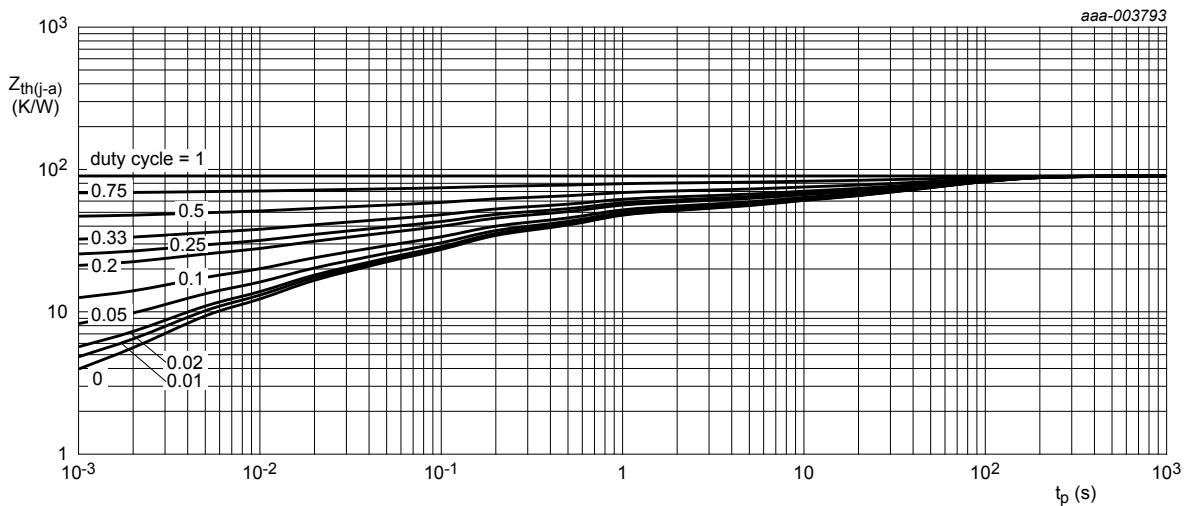


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics (per transistor)							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C		-20	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} =V _{GS} ; T _j = 25 °C		-0.45	-0.7	-0.95	V
I _{DSS}	drain leakage current	V _{DS} = -20 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-1	μA
		V _{DS} = -20 V; V _{GS} = 0 V; T _j = 150 °C		-	-	-10	μA
I _{GSS}	gate leakage current	V _{GS} = 8 V; V _{DS} = 0 V; T _j = 25 °C		-	-	10	μA
		V _{GS} = -8 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-10	μA
R _{DSon}	drain-source on-state resistance	V _{GS} = -4.5 V; I _D = -2 A; T _j = 25 °C		-	58	67	mΩ
		V _{GS} = -4.5 V; I _D = -2 A; T _j = 150 °C		-	82	95	mΩ
		V _{GS} = -2.5 V; I _D = -1.5 A; T _j = 25 °C		-	74	95	mΩ
		V _{GS} = -1.8 V; I _D = -1 A; T _j = 25 °C		-	97	137	mΩ
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -2 A; T _j = 25 °C		-	9	-	S
Dynamic characteristics (per transistor)							
Q _{G(tot)}	total gate charge	V _{DS} = -10 V; I _D = -2 A; V _{GS} = -4.5 V; T _j = 25 °C		-	6.3	9.5	nC
Q _{GS}	gate-source charge			-	1.2	-	nC
Q _{GD}	gate-drain charge			-	0.9	-	nC
C _{iss}	input capacitance	V _{DS} = -10 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	804	-	pF
C _{oss}	output capacitance			-	95	-	pF
C _{rss}	reverse transfer capacitance			-	66	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -10 V; I _D = -2 A; V _{GS} = -4.5 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	7	-	ns
t _r	rise time			-	15	-	ns
t _{d(off)}	turn-off delay time			-	41	-	ns
t _f	fall time			-	14	-	ns
Source-drain diode (per transistor)							
V _{SD}	source-drain voltage	I _S = -0.5 A; V _{GS} = 0 V; T _j = 25 °C		-	-0.7	-1.2	V

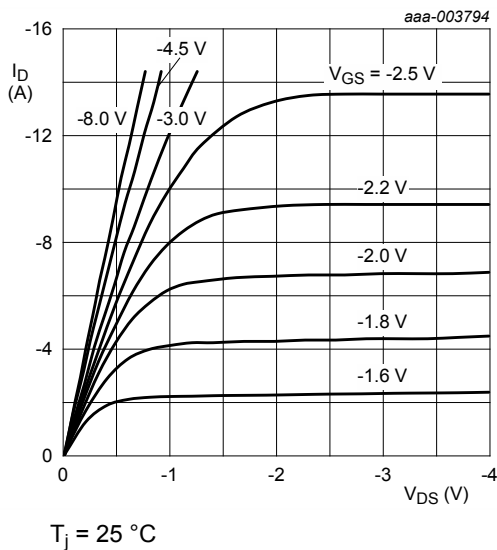


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

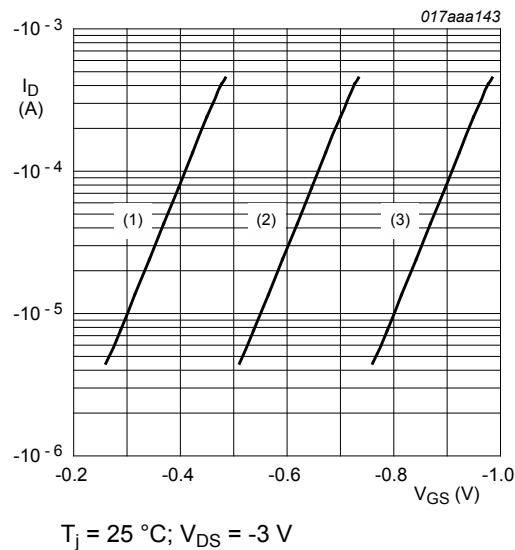


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

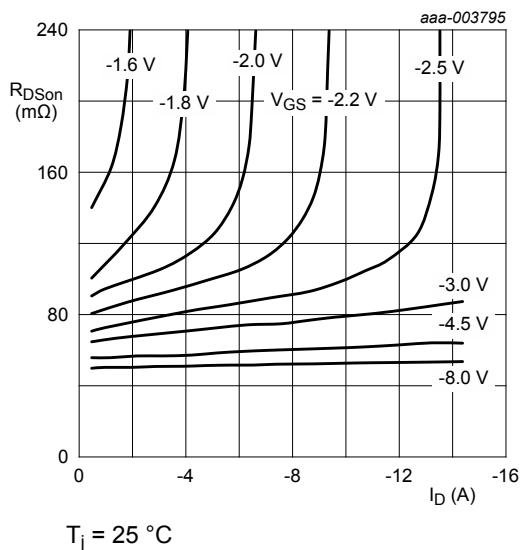


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

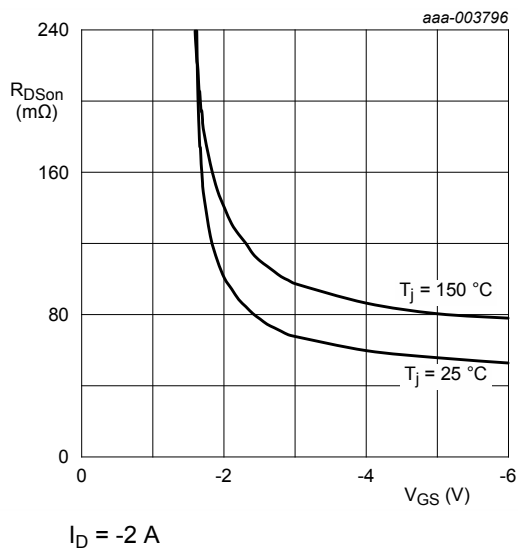


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

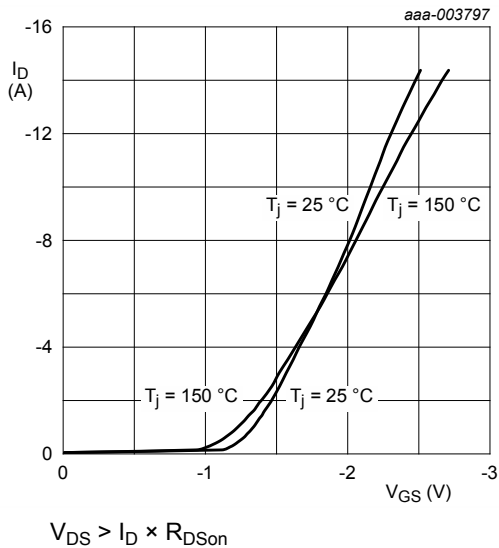


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

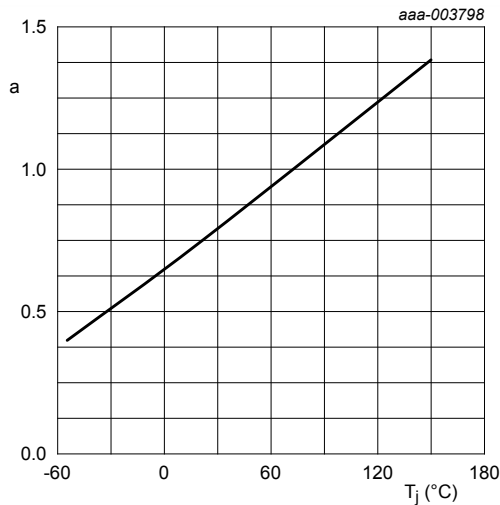


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

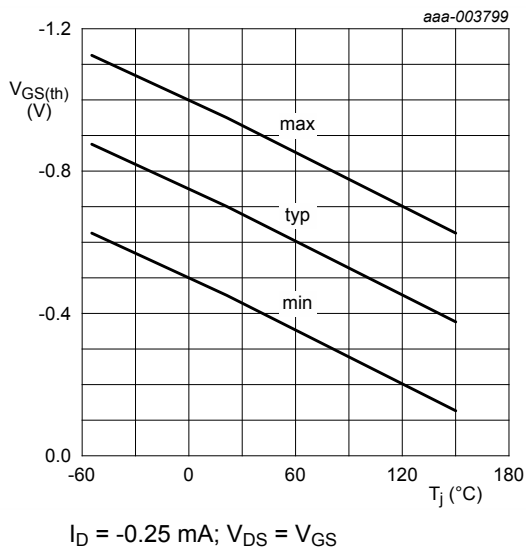


Fig. 12. Gate-source threshold voltage as a function of junction temperature

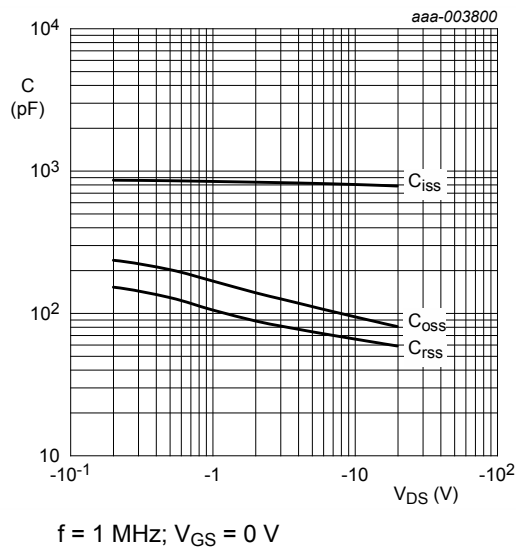


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

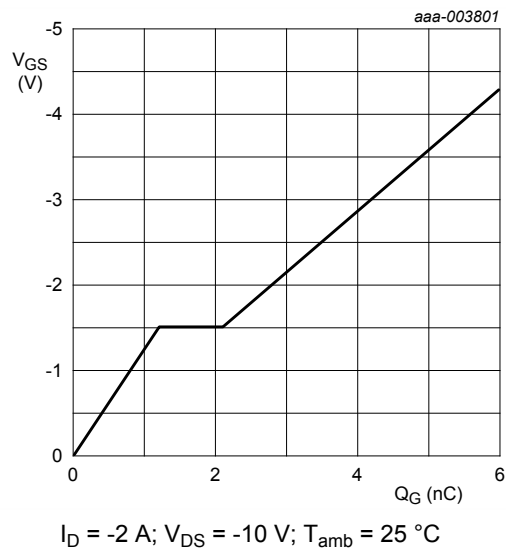


Fig. 14. Gate-source voltage as a function of gate charge; typical values

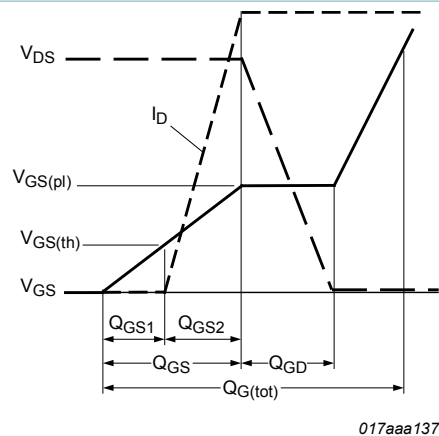
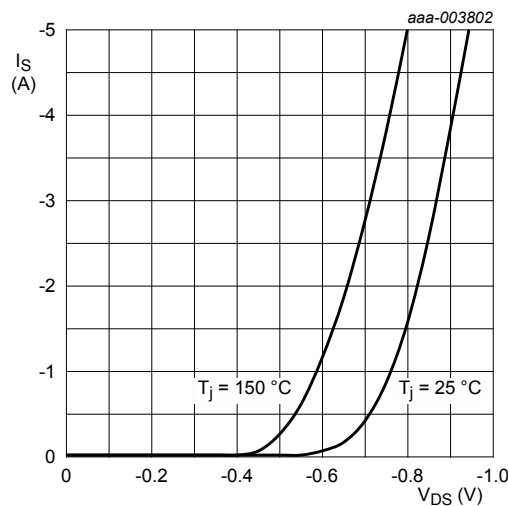


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

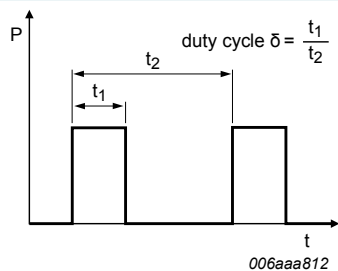
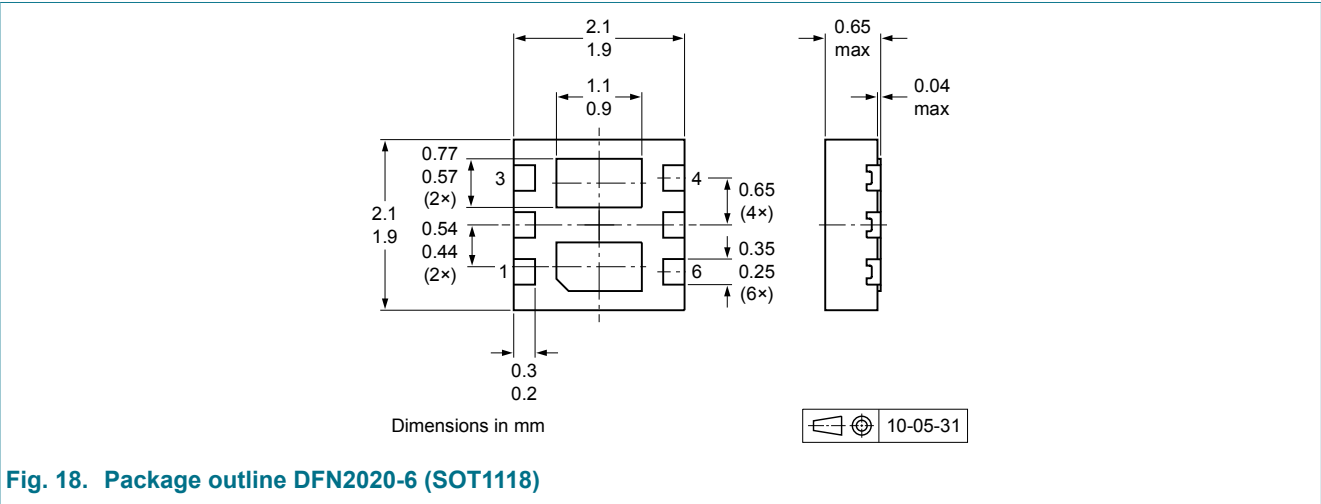
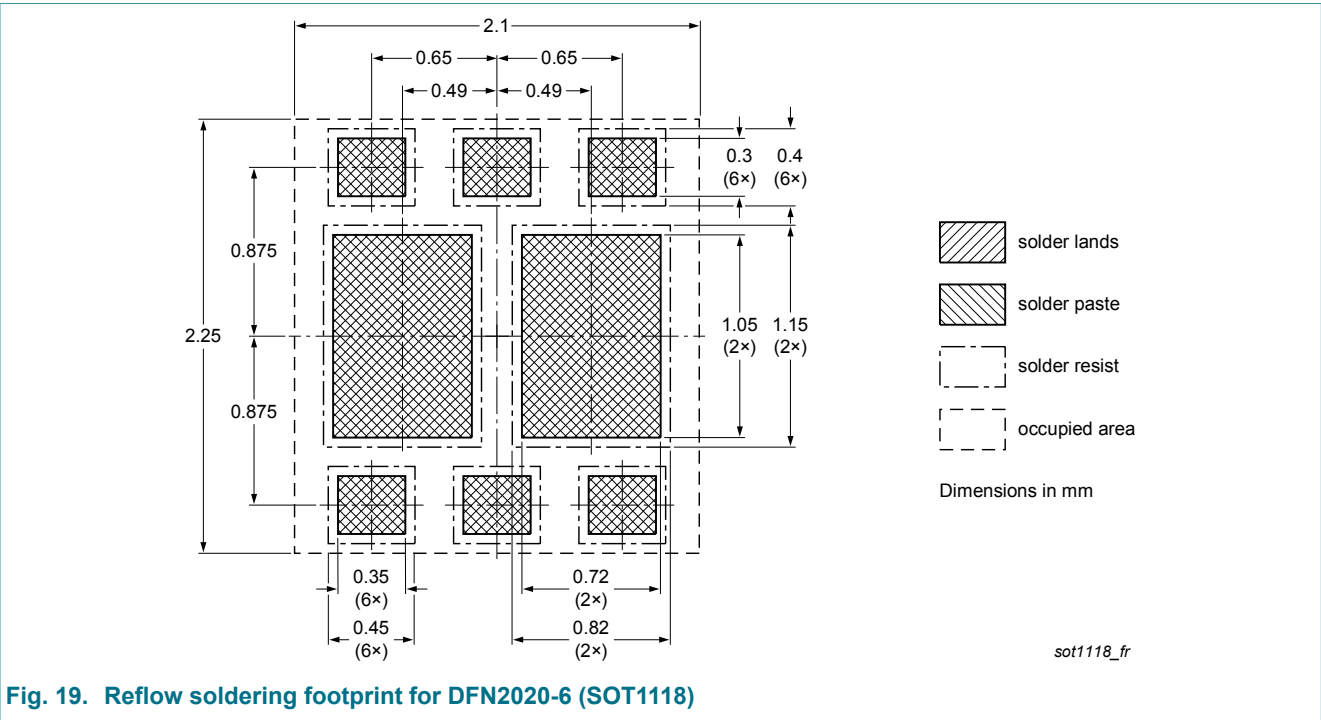


Fig. 17. Duty cycle definition

12. Package outline



13. Soldering



14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMDPB58UPE v.2	20160203	Product data sheet	-	PMDPB58UPE v.1
Modifications:	Figure 9: corrected			
PMDPB58UPE v.1	20120619	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
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