

# MC14051B, MC14052B, MC14053B



ON Semiconductor®

<http://onsemi.com>

## Analog Multiplexers/Demultiplexers

The MC14051B, MC14052B, and MC14053B analog multiplexers are digitally-controlled analog switches. The MC14051B effectively implements an SP8T solid state switch, the MC14052B a DP4T, and the MC14053B a Triple SPDT. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

### Features

- Triple Diode Protection on Control Inputs
- Switch Function is Break Before Make
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range ( $V_{DD} - V_{EE}$ ) = 3.0 to 18 V  
Note:  $V_{EE}$  must be  $\leq V_{SS}$
- Linearized Transfer Characteristics
- Low-noise –  $12 \text{ nV}/\sqrt{\text{Cycle}}$ ,  $f \geq 1.0 \text{ kHz}$  Typical
- Pin-for-Pin Replacement for CD4051, CD4052, and CD4053
- For 4PDT Switch, See MC14551B
- For Lower  $R_{ON}$ , Use the HC4051, HC4052, or HC4053 High-Speed CMOS Devices
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range (Referenced to $V_{EE}$ , $V_{SS} \geq V_{EE}$ )	-0.5 to +18.0	V
$V_{in}$ , $V_{out}$	Input or Output Voltage Range (DC or Transient) (Referenced to $V_{SS}$ for Control Inputs and $V_{EE}$ for Switch I/O)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient) per Control Pin	+10	mA
$I_{SW}$	Switch Through Current	$\pm 25$	mA
$P_D$	Power Dissipation per Package (Note 1)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$ ,  $V_{EE}$  or  $V_{DD}$ ). Unused outputs must be left open.

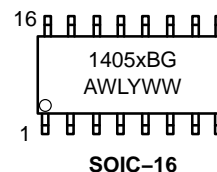


1  
SOIC-16  
D SUFFIX  
CASE 751B



1  
TSSOP-16  
DT SUFFIX  
CASE 948F

### MARKING DIAGRAMS



- x = 1, 2, or 3
- A = Assembly Location
- WL, L = Wafer Lot
- Y = Year
- WW, W = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

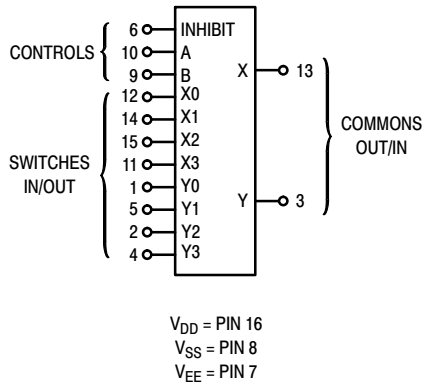
See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

# MC14051B, MC14052B, MC14053B

**MC14051B**  
8-Channel Analog  
Multiplexer/Demultiplexer



**MC14052B**  
Dual 4-Channel Analog  
Multiplexer/Demultiplexer



**MC14053B**  
Triple 2-Channel Analog  
Multiplexer/Demultiplexer



Note: Control Inputs referenced to V<sub>SS</sub>. Analog Inputs and Outputs reference to V<sub>EE</sub>. V<sub>EE</sub> must be ≤ V<sub>SS</sub>.

## PIN ASSIGNMENT



# MC14051B, MC14052B, MC14053B

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V <sub>DD</sub>	Test Conditions	-55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (Note 2)	Max	Min	Max	

### SUPPLY REQUIREMENTS (Voltages Referenced to V<sub>EE</sub>)

Power Supply Voltage Range	V <sub>DD</sub>	-	V <sub>DD</sub> - 3.0 ≥ V <sub>SS</sub> ≥ V <sub>EE</sub>	3.0	18	3.0	-	18	3.0	18	V	
Quiescent Current Per Package	I <sub>DD</sub>	5.0 10 15	Control Inputs: V <sub>in</sub> = V <sub>SS</sub> or V <sub>DD</sub> , Switch I/O: V <sub>EE</sub> ≤ V <sub>I/O</sub> ≤ V <sub>DD</sub> , and ΔV <sub>switch</sub> ≤ 500 mV (Note 3)	- - -	5.0 10 20	- - -	0.005 0.010 0.015	5.0 10 20	- - -	150 300 600	μA	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I <sub>D(AV)</sub>	5.0 10 15	T <sub>A</sub> = 25°C only (The channel component, (V <sub>in</sub> - V <sub>out</sub> )/R <sub>on</sub> , is not included.)	Typical						(0.07 μA/kHz) f + I <sub>DD</sub> (0.20 μA/kHz) f + I <sub>DD</sub> (0.36 μA/kHz) f + I <sub>DD</sub>		μA

### CONTROL INPUTS — INHIBIT, A, B, C (Voltages Referenced to V<sub>SS</sub>)

Low-Level Input Voltage	V <sub>IL</sub>	5.0 10 15	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	V
High-Level Input Voltage	V <sub>IH</sub>	5.0 10 15	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	- - -	3.5 7.0 11	- - -	V
Input Leakage Current	I <sub>in</sub>	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	-	±0.1	-	±0.00001	±0.1	-	1.0	μA
Input Capacitance	C <sub>in</sub>	-		-	-	-	5.0	7.5	-	-	pF

### SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y, Z (Voltages Referenced to V<sub>EE</sub>)

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V <sub>I/O</sub>	-	Channel On or Off	0	V <sub>DD</sub>	0	-	V <sub>DD</sub>	0	V <sub>DD</sub>	V <sub>PP</sub>
Recommended Static or Dynamic Voltage Across the Switch (Note 3) (Figure 5)	ΔV <sub>switch</sub>	-	Channel On	0	600	0	-	600	0	300	mV
Output Offset Voltage	V <sub>OO</sub>	-	V <sub>in</sub> = 0 V, No Load	-	-	-	10	-	-	-	μV
ON Resistance	R <sub>on</sub>	5.0 10 15	ΔV <sub>switch</sub> ≤ 500 mV (Note 3) V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control), and V <sub>in</sub> = 0 to V <sub>DD</sub> (Switch)	- - -	800 400 220	- - -	250 120 80	1050 500 280	- - -	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR <sub>on</sub>	5.0 10 15		- - -	70 50 45	- - -	25 10 10	70 50 45	- - -	135 95 65	Ω
Off-Channel Leakage Current (Figure 10)	I <sub>off</sub>	15	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel	-	±100	-	±0.05	±100	-	±1000	nA
Capacitance, Switch I/O	C <sub>I/O</sub>	-	Inhibit = V <sub>DD</sub>	-	-	-	10	-	-	-	pF
Capacitance, Common O/I	C <sub>O/I</sub>	-	Inhibit = V <sub>DD</sub> (MC14051B) (MC14052B) (MC14053B)	- - -	- - -	- - -	60 32 17	- - -	- - -	- - -	pF
Capacitance, Feedthrough (Channel Off)	C <sub>I/O</sub>	- -	Pins Not Adjacent Pins Adjacent	- -	- -	- -	0.15 0.47	- -	- -	- -	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

3. For voltage drops across the switch (ΔV<sub>switch</sub>) > 600 mV (> 300 mV at high temperature), excessive V<sub>DD</sub> current may be drawn, i.e. the current out of the switch may contain both V<sub>DD</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

# MC14051B, MC14052B, MC14053B

## ELECTRICAL CHARACTERISTICS (Note 4) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ ) ( $V_{EE} \leq V_{SS}$ unless otherwise indicated)

Characteristic	Symbol	$V_{DD} - V_{EE}$ Vdc	Typ (Note 5) All Types	Max	Unit
Propagation Delay Times (Figure 6) Switch Input to Switch Output ( $R_L = 1 \text{ k}\Omega$ ) MC14051 $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 26.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 11 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 9.0 \text{ ns}$ MC14052 $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 21.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 8.0 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 7.0 \text{ ns}$ MC14053 $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 16.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 4.0 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 3.0 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	35 15 12	90 40 30	ns
Inhibit to Output ( $R_L = 10 \text{ k}\Omega$ , $V_{EE} = V_{SS}$ ) Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level MC14051B	$t_{PHZ}, t_{PLZ},$ $t_{PZH}, t_{PZL}$	5.0 10 15	350 170 140	700 340 280	ns
MC14052B		5.0 10 15	300 155 125	600 310 250	ns
MC14053B		5.0 10 15	275 140 110	550 280 220	ns
Control Input to Output ( $R_L = 1 \text{ k}\Omega$ , $V_{EE} = V_{SS}$ ) MC14051B	$t_{PLH}, t_{PHL}$	5.0 10 15	360 160 120	720 320 240	ns
MC14052B		5.0 10 15	325 130 90	650 260 180	ns
MC14053B		5.0 10 15	300 120 80	600 240 160	ns
Second Harmonic Distortion ( $R_L = 10\text{K}\Omega$ , $f = 1 \text{ kHz}$ ) $V_{in} = 5 V_{PP}$	–	10	0.07	–	%
Bandwidth (Figure 7) ( $R_L = 50 \Omega$ , $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p, $C_L = 50\text{pF}$ $20 \text{ Log } (V_{out}/V_{in}) = -3 \text{ dB}$ )	BW	10	17	–	MHz
Off Channel Feedthrough Attenuation (Figure 7) $R_L = 1\text{K}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p $f_{in} = 4.5 \text{ MHz}$ — MC14051B $f_{in} = 30 \text{ MHz}$ — MC14052B $f_{in} = 55 \text{ MHz}$ — MC14053B	–	10	–50	–	dB
Channel Separation (Figure 8) ( $R_L = 1 \text{ k}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p, $f_{in} = 3.0 \text{ MHz}$ )	–	10	–50	–	dB
Crosstalk, Control Input to Common O/I (Figure 9) ( $R_1 = 1 \text{ k}\Omega$ , $R_L = 10 \text{ k}\Omega$ Control $t_{TLH} = t_{THL} = 20 \text{ ns}$ , Inhibit = $V_{SS}$ )	–	10	75	–	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14051B, MC14052B, MC14053B

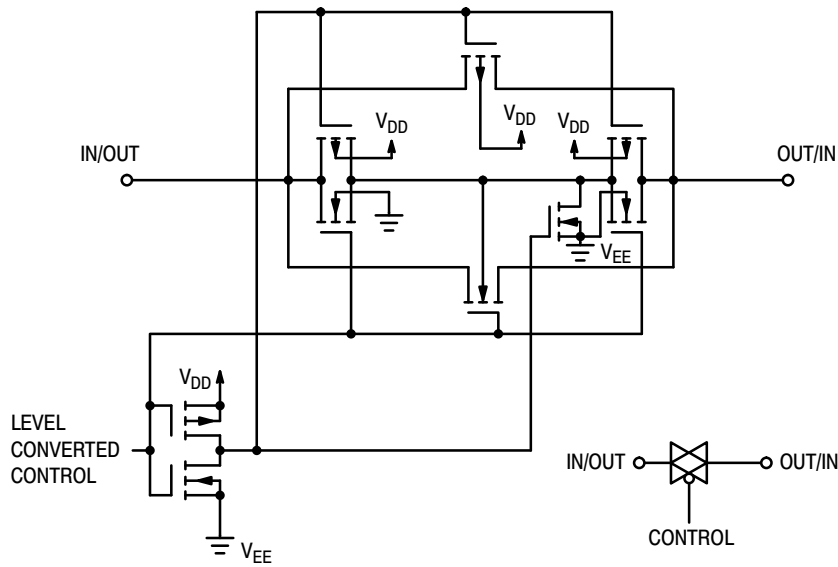


Figure 1. Switch Circuit Schematic

## TRUTH TABLE

Control Inputs			ON Switches		
Inhibit	Select		MC14051B	MC14052B	MC14053B
	C*	B A			
0	0	0 0	X0	Y0 X0	Z0 Y0 X0
0	0	0 1	X1	Y1 X1	Z0 Y0 X1
0	0	1 0	X2	Y2 X2	Z0 Y1 X0
0	0	1 1	X3	Y3 X3	Z0 Y1 X1
0	1	0 0	X4		Z1 Y0 X0
0	1	0 1	X5		Z1 Y0 X1
0	1	1 0	X6		Z1 Y1 X0
0	1	1 1	X7		Z1 Y1 X1
1	x	x x	None	None	None

\*Not applicable for MC14052  
x = Don't Care

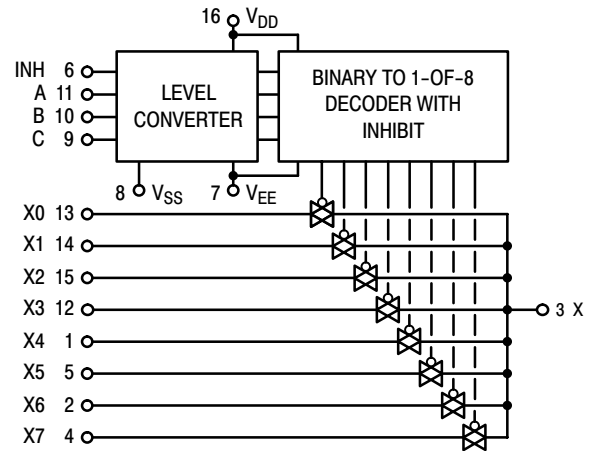


Figure 2. MC14051B Functional Diagram



Figure 3. MC14052B Functional Diagram



Figure 4. MC14053B Functional Diagram

TEST CIRCUITS



Figure 5.  $\Delta V$  Across Switch

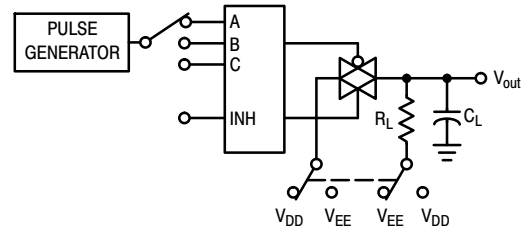


Figure 6. Propagation Delay Times, Control and Inhibit to Output

A, B, and C inputs used to turn ON or OFF the switch under test.



Figure 7. Bandwidth and Off-Channel Feedthrough Attenuation



Figure 8. Channel Separation (Adjacent Channels Used For Setup)



Figure 9. Crosstalk, Control Input to Common O/I



Figure 10. Off Channel Leakage

NOTE: See also Figures 7 and 8 in the MC14016B data sheet.

# MC14051B, MC14052B, MC14053B



Figure 11. Channel Resistance ( $R_{ON}$ ) Test Circuit

## TYPICAL RESISTANCE CHARACTERISTICS



Figure 12.  $V_{DD} = 7.5\text{ V}$ ,  $V_{EE} = -7.5\text{ V}$

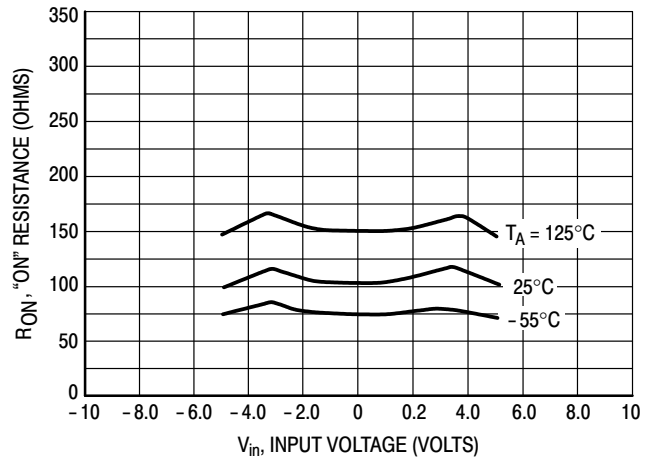


Figure 13.  $V_{DD} = 5.0\text{ V}$ ,  $V_{EE} = -5.0\text{ V}$



Figure 14.  $V_{DD} = 2.5\text{ V}$ ,  $V_{EE} = -2.5\text{ V}$

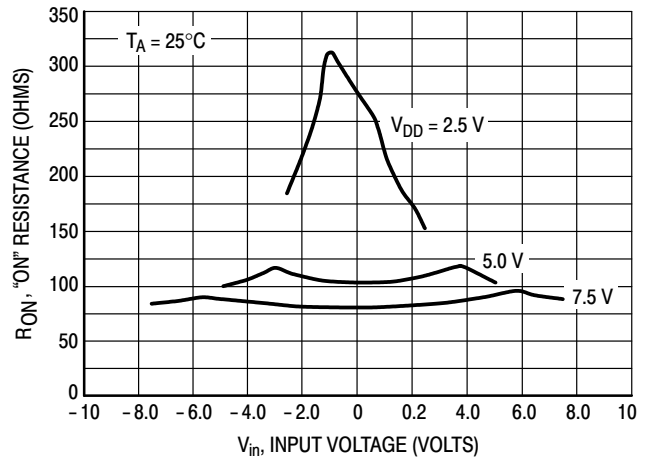


Figure 15. Comparison at  $25^\circ\text{C}$ ,  $V_{DD} = -V_{EE}$

APPLICATIONS INFORMATION

Figure A illustrates use of the on-chip level converter detailed in Figures 2, 3, and 4. The 0-to-5 V Digital Control signal is used to directly control a 9 V<sub>p-p</sub> analog signal.

The digital control logic levels are determined by V<sub>DD</sub> and V<sub>SS</sub>. The V<sub>DD</sub> voltage is the logic high voltage; the V<sub>SS</sub> voltage is logic low. For the example, V<sub>DD</sub> = +5 V = logic high at the control inputs; V<sub>SS</sub> = GND = 0 V = logic low.

The maximum analog signal level is determined by V<sub>DD</sub> and V<sub>EE</sub>. The V<sub>DD</sub> voltage determines the maximum recommended peak above V<sub>SS</sub>. The V<sub>EE</sub> voltage determines the maximum swing below V<sub>SS</sub>. For the example, V<sub>DD</sub> - V<sub>SS</sub> = 5 V maximum swing above V<sub>SS</sub>; V<sub>SS</sub> - V<sub>EE</sub> = 5 V maximum swing below V<sub>SS</sub>. The example shows a ±4.5 V signal which allows a 1/2 volt margin at each

peak. If voltage transients above V<sub>DD</sub> and/or below V<sub>EE</sub> are anticipated on the analog channels, external diodes (D<sub>X</sub>) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V<sub>DD</sub> and V<sub>EE</sub> is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V<sub>DD</sub> and V<sub>EE</sub>.

Balanced supplies are not required. However, V<sub>SS</sub> must be greater than or equal to V<sub>EE</sub>. For example, V<sub>DD</sub> = +10 V, V<sub>SS</sub> = +5 V, and V<sub>EE</sub> = -3 V is acceptable. See the Table below.



Figure A. Application Example

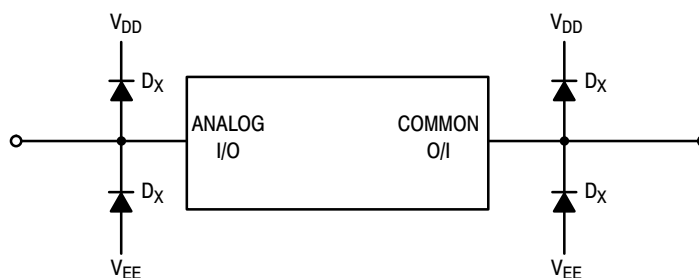


Figure B. External Germanium or Schottky Clipping Diodes

POSSIBLE SUPPLY CONNECTIONS

V <sub>DD</sub> In Volts	V <sub>SS</sub> In Volts	V <sub>EE</sub> In Volts	Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+8	0	-8	+8/0	+8 to -8 = 16 V <sub>p-p</sub>
+5	0	-12	+5/0	+5 to -12 = 17 V <sub>p-p</sub>
+5	0	0	+5/0	+5 to 0 = 5 V <sub>p-p</sub>
+5	0	-5	+5/0	+5 to -5 = 10 V <sub>p-p</sub>
+10	+5	-5	+10/ +5	+10 to -5 = 15 V <sub>p-p</sub>



## MC14051B, MC14052B, MC14053B

### ORDERING INFORMATION

Device	Package	Shipping†
MC14051BDG	SOIC-16 (Pb-Free)	48 Units / Rail
NLV14051BDG*	SOIC-16 (Pb-Free)	48 Units / Rail
MC14051BDR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
NLV14051BDR2G*	SOIC-16 (Pb-Free)	2500 / Tape & Reel
MC14051BDTR2G	TSSOP-16 (Pb-Free)	2500 / Tape & Reel
NLV14051BDTR2G*	TSSOP-16 (Pb-Free)	2500 / Tape & Reel

MC14052BDG	SOIC-16 (Pb-Free)	48 Units / Rail
NLV14052BDG*	SOIC-16 (Pb-Free)	48 Units / Rail
MC14052BDR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
NLV14052BDR2G*	SOIC-16 (Pb-Free)	2500 / Tape & Reel
MC14052BDTR2G	TSSOP-16 (Pb-Free)	2500 / Tape & Reel
NLV14052BDTR2G*	TSSOP-16 (Pb-Free)	2500 / Tape & Reel

MC14053BDG	SOIC-16 (Pb-Free)	48 Units / Rail
NLV14053BDG*	SOIC-16 (Pb-Free)	48 Units / Rail
MC14053BDR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
NLV14053BDR2G*	SOIC-16 (Pb-Free)	2500 / Tape & Reel
MC14053BDTR2G	TSSOP-16 (Pb-Free)	2500 / Tape & Reel
NLV14053BDTR2G*	TSSOP-16 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

## SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- |  |  |  |  |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p>                           | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p>   | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p>                                 | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> |  |

### SOLDERING FOOTPRINT



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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-16  
CASE 948F-01  
ISSUE B

DATE 19 OCT 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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