NCN2411

4-Channel Differential 1:2 Mux/Demux Switch for PCI Express Gen2

The NCN2411 is a 4−Channel differential SPDT switch designed to route PCI Express Gen2 signals. When used in a PCI Express application, the switch can handle up to two PCIe lanes. Due to the ultra−low ON−state capacitance (2 pF typ) and resistance (7.5 Ω typ), this switch is ideal for switching high frequency signals up to a signal bit rate (BR) of 5 Gbps. This switch pinout is designed to be used in BTX form factor desktop PCs and is available in a space−saving 3.5x9x0.75 mm WQFN42 package.

Features

- V_{DD} Power Supply from 1.5 V to 2.0 V
- 4 Differential Channels 2:1 MUX/DEMUX
- Compatible with PCIe 2.0
- Data Rate: Supports 5 Gbps
- Low Crosstalk: −30 dB @ 3 GHz
- Low Bit−to−Bit Skew: 5 ps
- Low R_{ON} Resistance: 13 Ω max
- Low C_{ON} Capacitance: 2 pF
- Low Supply Current: 200 μA
- Insertion Loss: −2 dB @ 3 GHz
- Space Saving, Small WQFN−42 Package
- This is a Pb−Free Device

Typical Applications

- Notebook Computer
- Desktop computer
- Server/Storage Area Network

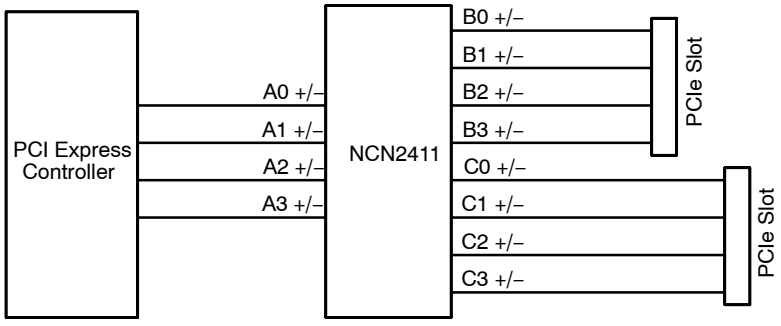
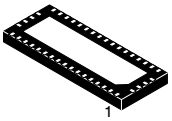


Figure 1. Application Schematic

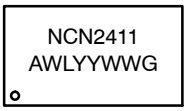
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WQFN42
CASE 510AP

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCN2411MTTWG	WQFN42 (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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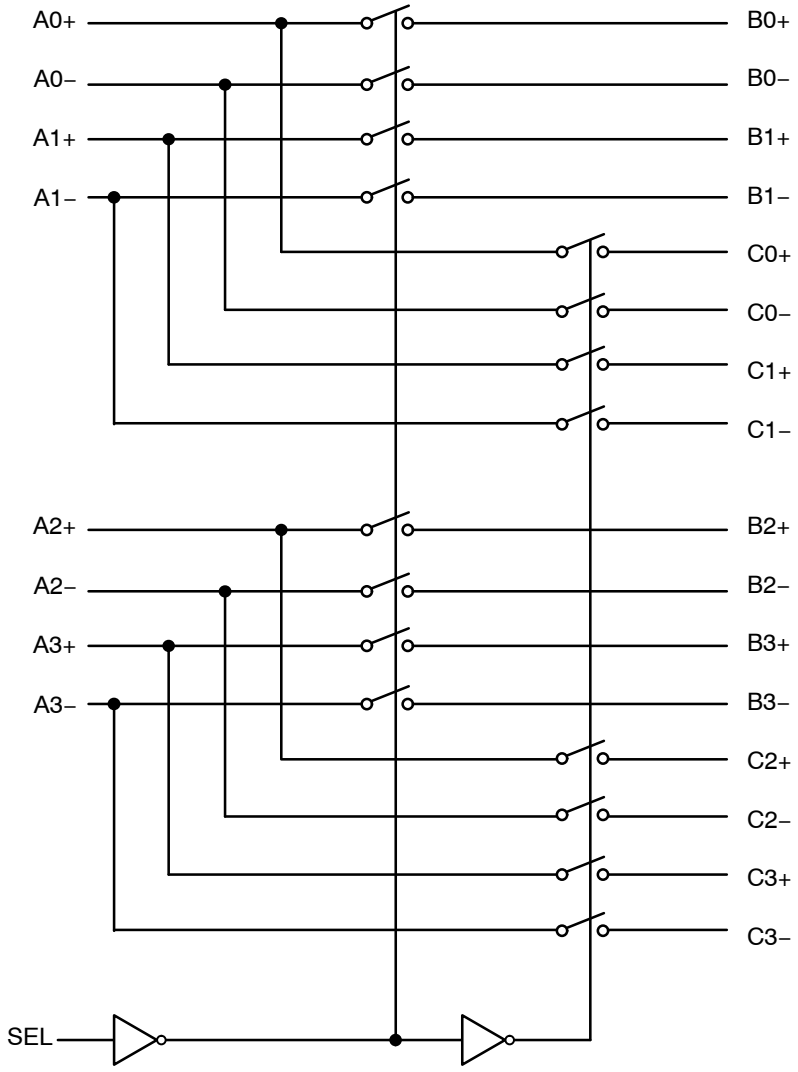


Figure 2. NCN2411 Functional Block Diagram (Top View)

TRUTH TABLE

Function	SEL
A_N to B_N	L
A_N to C_N	H

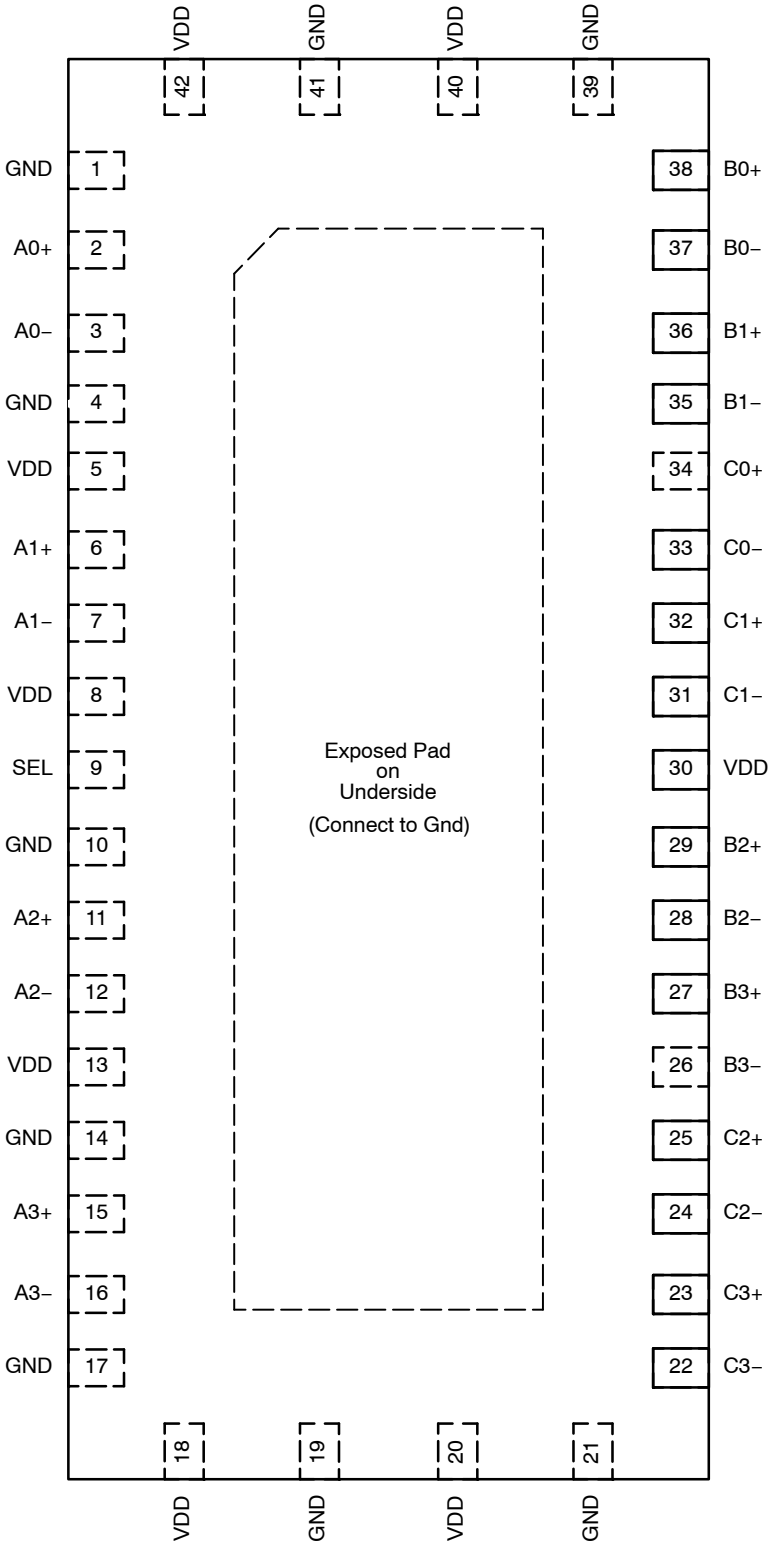


Figure 3. Pin Description
(Top View)

PIN FUNCTION AND DESCRIPTION

Pin	Pin Name	Description
2, 3	A0+, A0−	Signal I/0, Channel 0, Port A
6, 7	A1+, A1−	Signal I/0, Channel 1, Port A
11, 12	A2+, A2−	Signal I/0, Channel 2, Port A
15, 16	A3+, A3−	Signal I/0, Channel 3, Port A
38, 37	B0+, B0−	Signal I/0, Channel 0, Port B
36, 35	B1+, B1−	Signal I/0, Channel 1, Port B
29, 28	B2+, B2−	Signal I/0, Channel 2, Port B
27, 26	B3+, B3−	Signal I/0, Channel 3, Port B
34, 33	C0+, C0−	Signal I/0, Channel 0, Port C
32, 31	C1+, C1−	Signal I/0, Channel 1, Port C
25, 24	C2+, C2−	Signal I/0, Channel 2, Port C
23, 22	C3+, C3−	Signal I/0, Channel 3, Port C
9	SEL	Operational Mode Select (When SEL = 0: A → B, When SEL = 1: A → C) Do not float this pin.
5, 8, 13, 18, 20, 30, 40, 42	VDD	DC Supply: 1.5 V to 2.0 V
1, 4, 10, 14, 17, 19, 21, 39, 41	GND	Power Ground
Exposed Pad	−	The exposed pad on the backside of package is internally connected to GND. Externally the pad should also be user−connected to GND.

MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Power Supply Voltage	V_{DD}	−0.5 to 2.5	V_{DC}
Input/Output Voltage Range of the Switch (A_N, B_N, C_N)	V_{IS}	−0.5 to V_{DD}	V_{DC}
Selection Pin Voltages	V_{SEL}	−0.5 to V_{DD}	V_{DC}
Continuous Current Through One Switch	I_{cc}	±120	mA
Maximum Junction Temperature (Note 1)	T_J	150	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	75	°C/W
Latch−up Current (Note 2)	I_{LU}	±100	mA
Human Body Model (HBM) ESD Rating (Note 3)	ESD HBM	7000	V
Machine Model (MM) ESD Rating (Note 3)	ESD MM	400	V
Moisture Sensitivity (Note 4)	MSL	Level 1	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.
2. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78.
3. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±7.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±400 V per JEDEC standard: JESD22−A115 for all pins.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (T_A = −40°C to +85°C, V_{DD} = 1.5 V to 2.0 V, GND = 0V)

Symbol	Pins	Parameters	Conditions (Note 5)	Min.	Typ (Note 6)	Max.	Units
POWER SUPPLY							
V_{DD}	V_{DD}, GND	Supply Voltage Range	With respect to GND	1.5	1.8	2.0	V
I_{DD}	V_{DD}, GND	Quiescent Supply Current	V_{DD} = 2 V, V_{SEL} = GND or V_{DD}		200	300	μA
DATA SWITCH PERFORMANCE							
V_{IS}	A_N, B_N, C_N	Data Input/Output Voltage Range		0		1.2	V
R_{ON}	B_N	On Resistance (B_N)	V_{DD} = 1.5 V, V_{IS} = 0 V to 1.2 V, I_{IS} = 15 mA		7.5	13	Ω
R_{ON}	C_N	On Resistance (C_N)	V_{DD} = 1.5 V, V_{IS} = 0 V to 1.2 V, I_{IS} = 15 mA		8.0	13	Ω
$R_{ON(flat)}$	B_N	On Resistance Flatness	V_{DD} = 1.5 V, V_{IS} = 0 V to 1.2 V, I_{IS} = 15 mA (Note 7)		0.1	1.24	Ω
$R_{ON(flat)}$	C_N	On Resistance Flatness	V_{DD} = 1.5 V, V_{IS} = 0 V to 1.2 V, I_{IS} = 15 mA (Note 7)		0.1	1.24	Ω
ΔR_{ON}	B_N	On Resistance Matching(B_N)	V_{DD} = 1.5 V, V_{IS} = 0 V, I_{IS} = 15 mA (Note 7)			0.35	Ω
ΔR_{ON}	C_N	On Resistance Matching(C_N)	V_{DD} = 1.5 V, V_{IS} = 0 V, I_{IS} = 15 mA (Note 7)			0.35	Ω
C_{ON}	A_N to B_N, A_N to C_N	On Capacitance	f = 1 MHz, Switch On, Open Output		2.0		pF
C_{OFF}	A_N to B_N, A_N to C_N	Off Capacitance	f = 1 MHz, Switch Off		1.5		pF
I_{ON}	A_N to B_N, A_N to C_N	On Leakage Current	V_{DD} = 2 V, V_{AN} = 0 V, 1.2 V, Switch On to B_N/C_N, B_N/C_N pins are unconnected	−1		+1	μA
I_{OFF}	A_N to B_N, A_N to C_N	Off Leakage Current	V_{DD} = 2 V, V_{AN} = 0 V, 1.2 V, Switch Off to B_N/C_N, V_{BN}/V_{CN} = 1.2 V, 0 V	−1		+1	μA
LOGIC INPUT CHARACTERISTICS (SEL Pin)							
V_{IH}	SEL	Input HIGH Voltage	(Note 7)	0.65 x V_{DD}		V_{DD}	V
V_{IL}	SEL	Input LOW Voltage	(Note 7)	0		0.35 x V_{DD}	V
V_{IK}	SEL	Clamp Diode Voltage	V_{DD} = Max, I_{SEL} = −18mA		−0.7	−1.2	V
I_{IH}	SEL	Input HIGH Current	V_{DD} = Max, V_{SEL} = V_{DD}			±5	μA
I_{IL}	SEL	Input LOW Current	V_{DD} = Max, V_{SEL} = GND			±5	μA
SWITCHING CHARACTERISTICS							
t_{SELON}	SEL, A_N, B_N/C_N	Line Enable Time	SEL to A_N, B_N, C_N R_L = 50 Ω, C_L = 20 pF		8.0		ns
t_{SELOFF}	SEL, A_N, B_N/C_N	Line Disable Time	SEL to A_N, B_N, C_N R_L = 50 Ω, C_L = 20 pF		5.0		ns
t_{b-b}	A_N, B_N/C_N	Bit−to−bit skew	Within the same differential pair		9.0		ps
t_{ch-ch}	A_N, B_N	Channel−to channel skew	Maximum skew between all channels		50		ps

5. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
6. Typical values are at V_{DD} = 1.8 V, T_A = 25°C ambient and maximum loading.
7. Guaranteed by design and/or characterization.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (T_A = −40°C to +85°C, V_{DD} = 1.5 V to 2.0 V, GND = 0V)

Symbol	Pins	Parameters	Conditions (Note 5)	Min.	Typ (Note 6)	Max.	Units
DYNAMIC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE							
BR	A_N to B_N, A_N to C_N	Signal Bit Rate			5.0		Gbps
D_{IL}	A_N to B_N, A_N to C_N	Differential Insertion Loss	f = 3 GHz		−2.0		dB
			f = 100 MHz		−0.7		dB
D_{CTK}	A_N, B_N, C_N	Differential Crosstalk	f = 3 GHz		−30		dB
			f = 100 MHz		−58		dB
D_{ISO}	A_N to B_N, A_N to C_N	Differential Off Isolation	f = 3 GHz		−23		dB
			f = 100 MHz		−58		dB
D_{RL}	A_N to B_N, A_N to C_N	Differential Return Loss	f = 3 GHz		−6.0		dB
			f = 100 MHz		−22		dB

5. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
6. Typical values are at V_{DD} = 1.8 V, T_A = 25°C ambient and maximum loading.
7. Guaranteed by design and/or characterization.

TYPICAL OPERATING CHARACTERISTICS

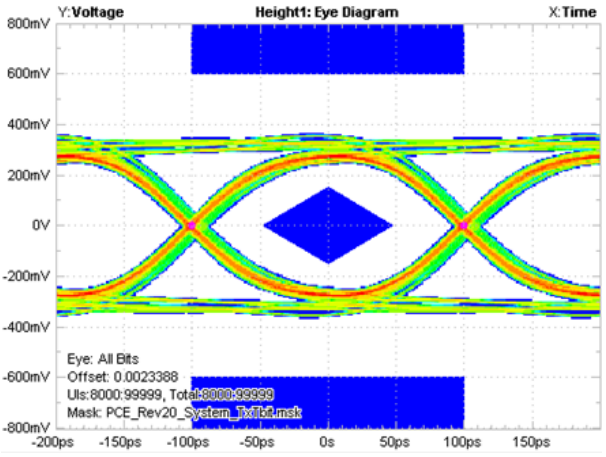


Figure 4. PCI Express Eye Diagram at 5 Gbps, 800 mVpp Differential Swing (Minimum Case)

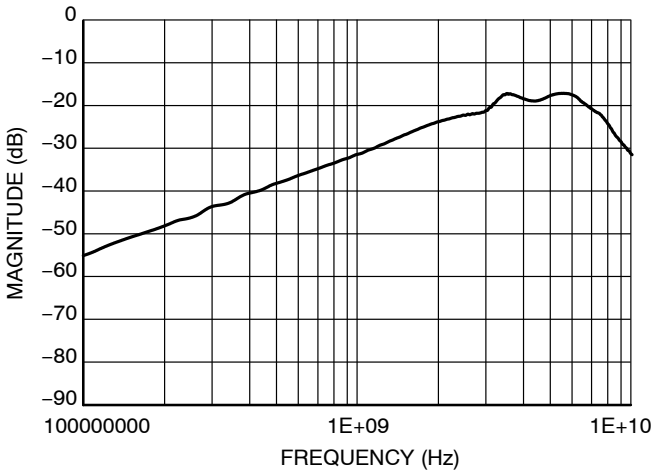


Figure 5. Differential Off Isolation

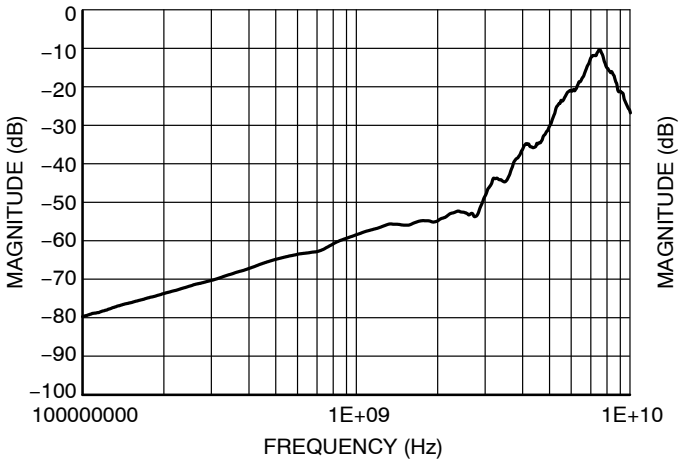


Figure 6. Differential Crosstalk

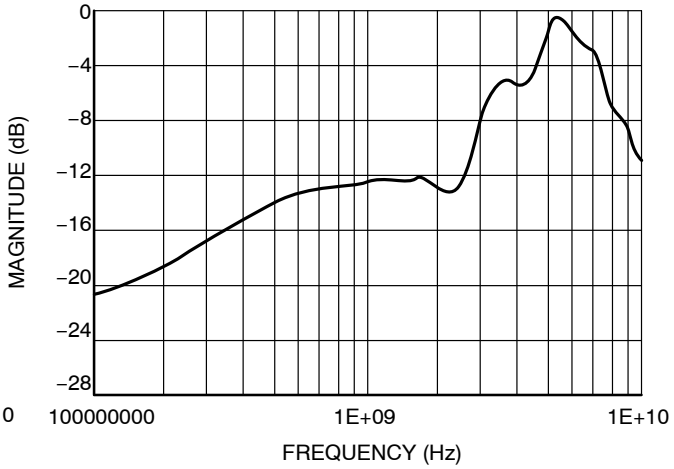


Figure 7. Differential Return Loss

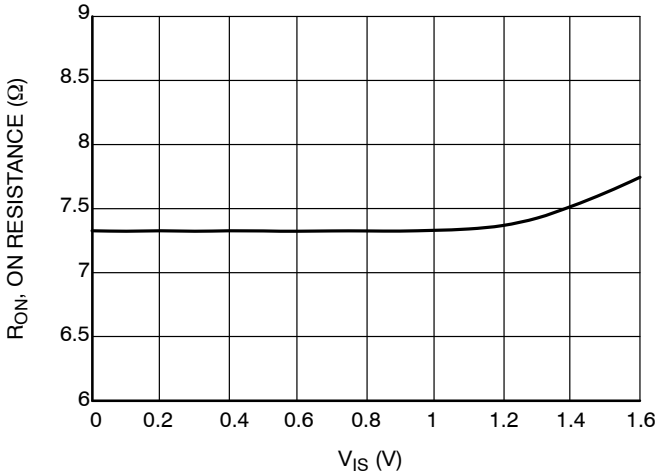


Figure 8. R_{ON} vs. V_{IS}

PARAMETER MEASUREMENT INFORMATION

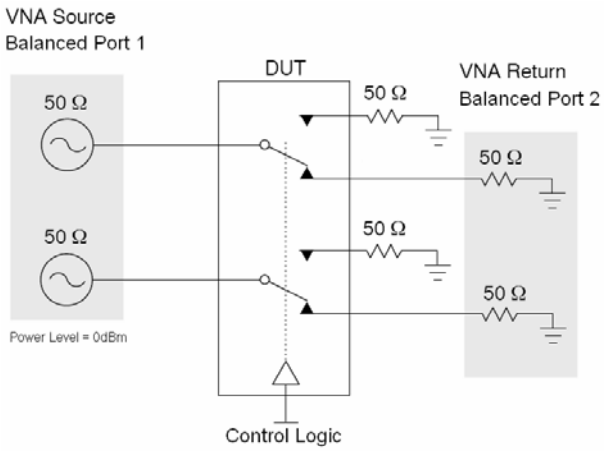


Figure 9. Differential Insertion Loss (S_{DD21}) and Differential Return Loss (S_{DD11})

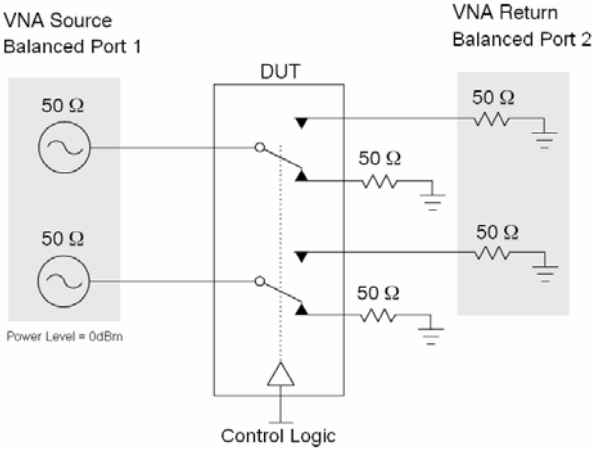


Figure 10. Differential Off Isolation (S_{DD21})

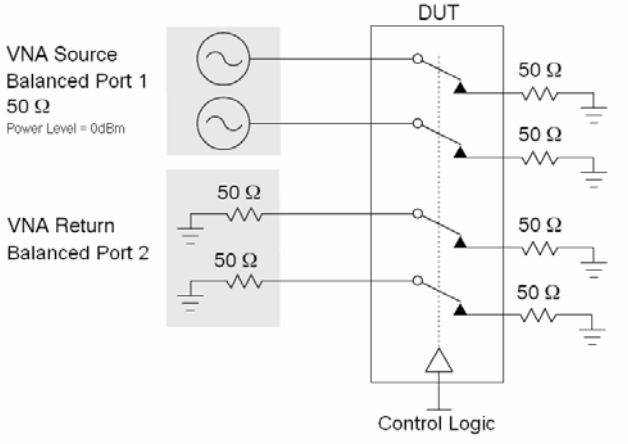
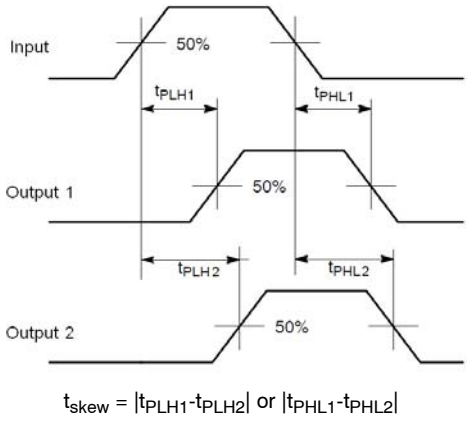
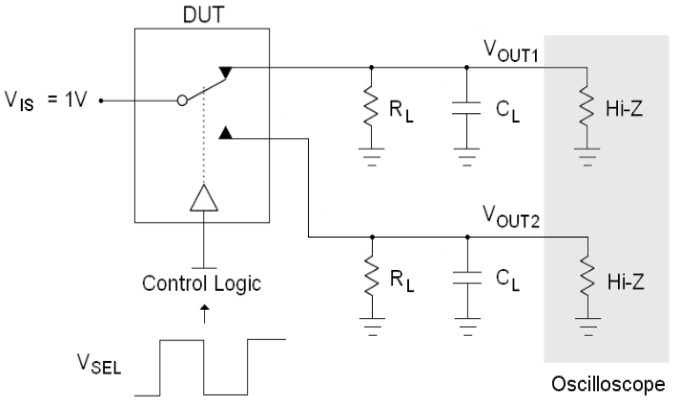


Figure 11. Differential Crosstalk (S_{DD21})



$t_{skew} = |t_{PLH1}-t_{PLH2}|$ or $|t_{PHL1}-t_{PHL2}|$

Figure 12. Bit−to−Bit and Channel−to−Channel Skew



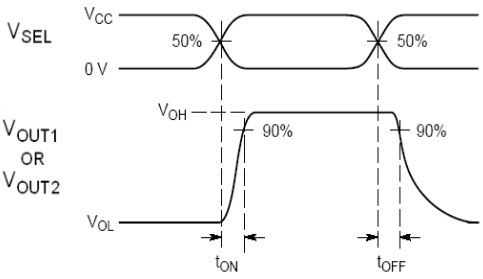


Figure 13. t_{ON} and t_{OFF}

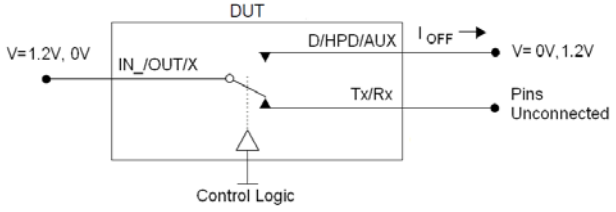


Figure 14. Off State Leakage

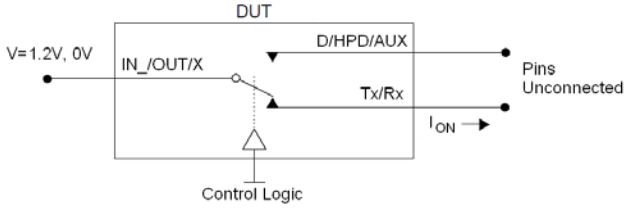


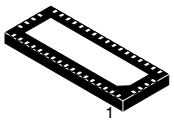
Figure 15. On State Leakage

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

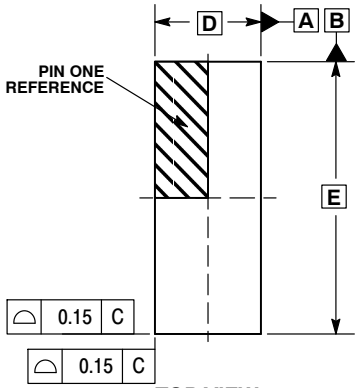
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WQFN42 3.5x9, 0.5P
CASE 510AP−01
ISSUE O

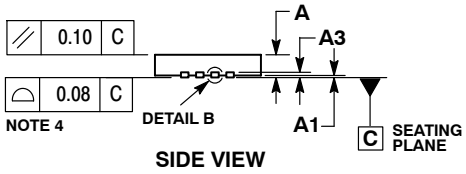
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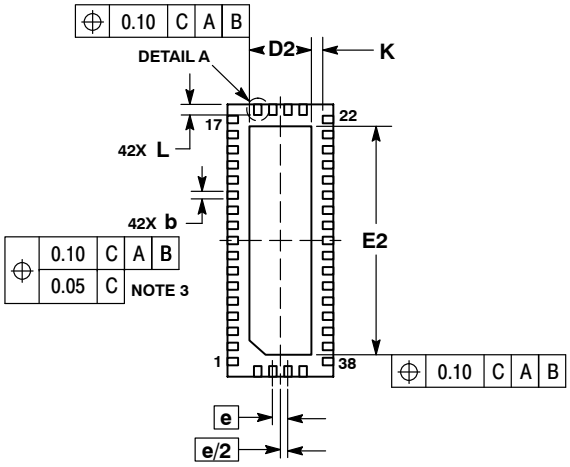
SCALE 2:1



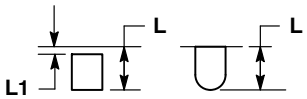
TOP VIEW



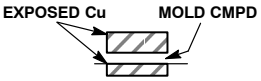
SIDE VIEW



BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

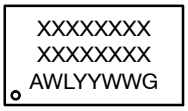


DETAIL B
ALTERNATE CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	3.50 BSC	
D2	1.95	2.15
E	9.00 BSC	
E2	7.45	7.65
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.50
L1	0.00	0.15

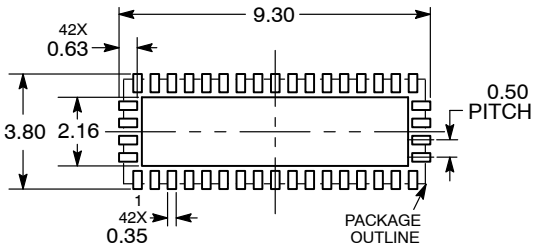
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	WQFN42 3.5X9, 0.5P	PAGE 1 OF 1

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