Dual Common Base-Collector Bias Resistor Transistors

NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base–emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the EMC2DXV5T1G series, two complementary BRT devices are housed in the SOT–553 package which is ideal for low power surface mount applications where board space is at a premium.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Devices

MAXIMUM RATINGS ($T_A = 25^{\circ}C$ unless otherwise noted, common for Q_1 and Q_2 , — minus sign for Q_1 (PNP) omitted)

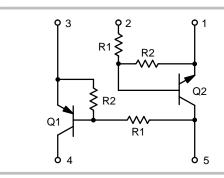
2. 0 1()			
Rating	Symbol	Value	Unit
Collector-Base Voltage	V _{CBO}	50	Vdc
Collector-Emitter Voltage	V _{CEO}	50	Vdc
Collector Current	Ιc	100	mAdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



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SOT-553 CASE 463B

MARKING DIAGRAM



Ux = Specific Device Code

x = C, 3, E, or 5

M = Date Code

= Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
ONE JUNCTION HEATED			
Total Device Dissipation $T_A = 25^{\circ}C$ Derate above 25°C	P _D	357 (Note 1) 2.9 (Note 1)	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{ hetaJA}$	350 (Note 1)	°C/W
BOTH JUNCTIONS HEATED			
Total Device Dissipation $ T_A = 25^{\circ} C $ Derate above $25^{\circ} C$	P _D	500 (Note 1) 4.0 (Note 1)	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{ heta JA}$	250 (Note 1)	°C/W
Junction and Storage Temperature	T _J , T _{stq}	-55 to +150	°C

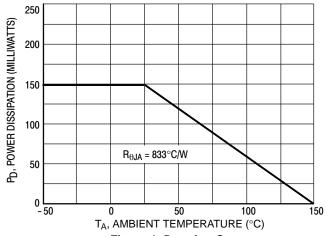
^{1.} FR-4 @ Minimum Pad

DEVICE ORDERING INFORMATION, MARKING AND RESISTOR VALUES

		Transisto	r 1 – PNP	Transisto	r 2 – NPN		
Device	Marking	R1 (K)	R2 (K)	R1 (K)	R2 (K)	Package	Shipping [†]
EMC2DXV5T1G	UC	22	22	22	22		4000 / Tape & Reel
NSVEMC2DXV5T1G*	UC	22	22	22	22		4000 / Tape & Reel
EMC3DXV5T1G	Ш	40	40	40	40	SOT-553	4000 / Tape & Reel
EMC3DXV5T5G	U3	10	10	10	10	(Pb-Free)	8000 / Tape & Reel
EMC4DXV5T1G	UE	10	47	47	47		4000 / Tape & Reel
EMC5DXV5T1G	U5	4.7	10	47	47		4000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
Q1 TRANSISTOR: PNP OFF CHARACTERISTICS					
Collector-Base Cutoff Current (V _{CB} = 50 V, I _E = 0)	I _{CBO}	_	_	100	nAdc
Collector-Emitter Cutoff Current (V _{CB} = 50 V, I _B = 0)	I _{CEO}	-	-	500	nAdc
		- - - -	- - - -	0.2 0.5 0.2 1.0	mAdc
ON CHARACTERISTICS					
Collector-Base Breakdown Voltage ($I_C = 10 \mu A, I_E = 0$)	$V_{(BR)CBO}$	50	-	-	Vdc
Collector-Emitter Breakdown Voltage (I _C = 2.0 mA, I _B = 0)	V _{(BR)CEO}	50	-	-	Vdc
$ \begin{array}{lll} \text{DC Current Gain} & \text{EMC2DXV5T1G} \\ \text{(V_{CE} = 10 V, I_{C} = 5.0 mA)} & \text{EMC3DXV5T1G} \\ & \text{EMC4DXV5T1G} \\ & \text{EMC5DXV5T1G} \\ \end{array} $		60 35 80 20	100 60 140 35	- - - -	
Collector–Emitter Saturation Voltage (I _C = 10 mA, I _B = 0.3 mA)	V _{CE(SAT)}	-	-	0.25	Vdc
Output Voltage (on) (V _{CC} = 5.0 V, V _B = 2.5 V, R _L = 1.0 k Ω)	V _{OL}	-	-	0.2	Vdc
Output Voltage (off) (V _{CC} = 5.0 V, V _B = 0.5 V, R _L = 1.0 k Ω)	V _{OH}	4.9	-	-	Vdc
Input Resistor EMC2DXV5T1G EMC3DXV5T1G, EMC4DXV5T1G EMC5DXV5T1G		15.4 7.0 3.3	22 10 4.7	28.6 13 6.1	kΩ
Resistor Ratio EMC2DXV5T1G EMC3DXV5T1G EMC4DXV5T1G EMC5DXV5T1G EMC5DXV5T1G		0.8 0.8 0.17 0.38	1.0 1.0 0.21 0.47	1.2 1.2 0.25 0.56	
Q2 TRANSISTOR: NPN OFF CHARACTERISTICS					
Collector-Base Cutoff Current ($V_{CB} = 50 \text{ V}, I_{E} = 0$)	I _{CBO}	-	-	100	nAdc
Collector-Emitter Cutoff Current (V _{CB} = 50 V, I _B = 0)	I _{CEO}	-	-	500	nAdc
	LBO	- - -	- - -	0.2 0.5 0.1	mAdc
ON CHARACTERISTICS		•	1	•	•
Collector-Base Breakdown Voltage ($I_C = 10 \mu A, I_E = 0$)	V _{(BR)CBO}	50	-	-	Vdc
Collector-Emitter Breakdown Voltage (I _C = 2.0 mA, I _B = 0)	V _{(BR)CEO}	50	-	-	Vdc
DC Current Gain EMC2DXV5T1G $(V_{CE} = 10 \text{ V}, I_C = 5.0 \text{ mA})$ EMC4DXV5T1G, EMC5DXV5T1G EMC4DXV5T1G, EMC5DXV5T1G	, -	60 35 80	100 60 140	- - -	
Collector–Emitter Saturation Voltage (I _C = 10 mA, I _B = 0.3 mA)	V _{CE(SAT)}	-	-	0.25	Vdc
Output Voltage (on) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 k Ω)	V _{OL}	_	_	0.2	Vdc
Output Voltage (off) (V _{CC} = 5.0 V, V _B = 0.5 V, R _L = 1.0 k Ω)	V _{OH}	4.9	_	-	Vdc
Input Resistor EMC2DXV5T1G EMC3DXV5T1G EMC4DXV5T1G, EMC5DXV5T1G		15.4 7.0 33	22 10 47	28.6 13 61	kΩ
Resistor Ratio EMC2DXV5T1G EMC3DXV5T1G		0.8 0.8	1.0 1.0	1.2 1.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL ELECTRICAL CHARACTERISTICS - EMC2DXV5T1 PNP TRANSISTOR

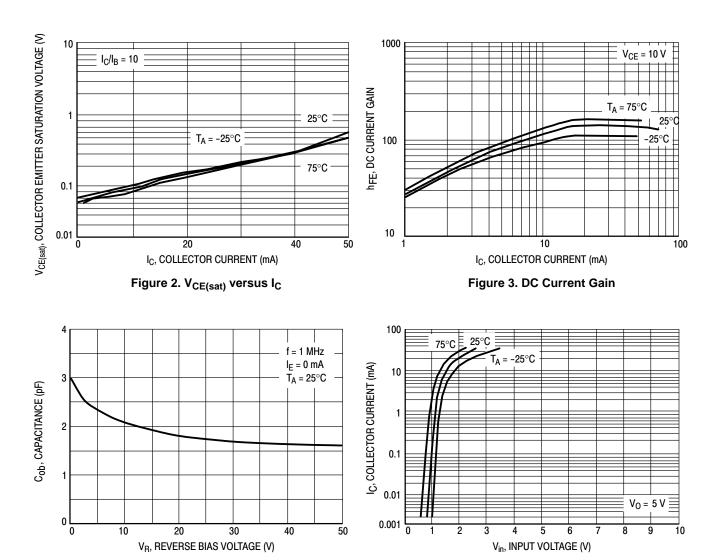


Figure 4. Output Capacitance

Figure 5. Output Current versus Input Voltage

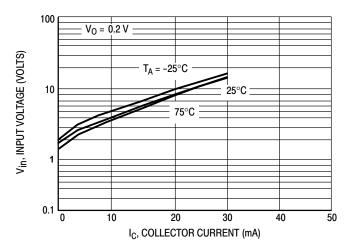
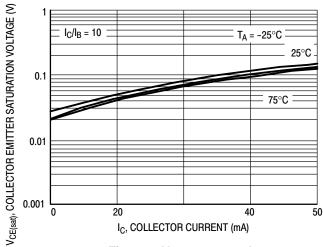


Figure 6. Input Voltage versus Output Current

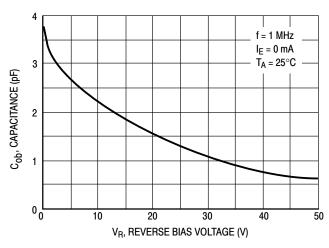
TYPICAL ELECTRICAL CHARACTERISTICS - EMC2DXV5T1 NPN TRANSISTOR



1000 V_{CE} = 10 V T_A = 75°C 25°C 25°C 25°C 100 T_C, COLLECTOR CURRENT (mA)

Figure 7. $V_{CE(sat)}$ versus I_C

Figure 8. DC Current Gain



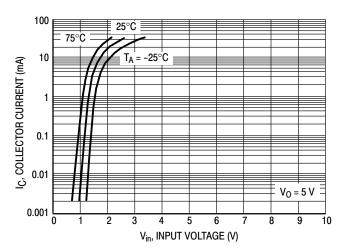


Figure 9. Output Capacitance

Figure 10. Output Current versus Input Voltage

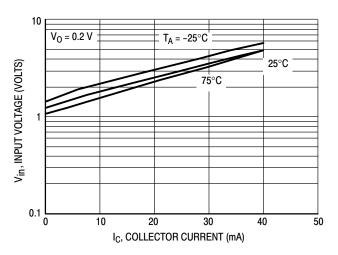


Figure 11. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS - EMC3DXV5T1 PNP TRANSISTOR

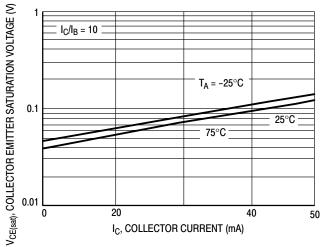


Figure 12. V_{CE(sat)} versus I_C

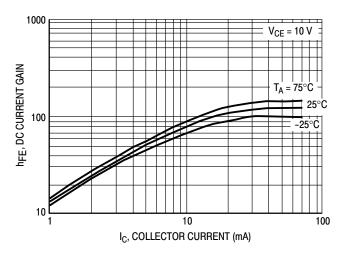


Figure 13. DC Current Gain

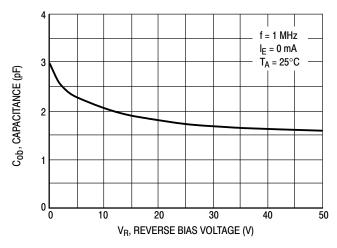


Figure 14. Output Capacitance

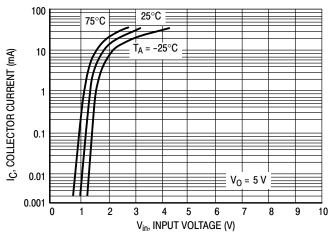


Figure 15. Output Current versus Input Voltage

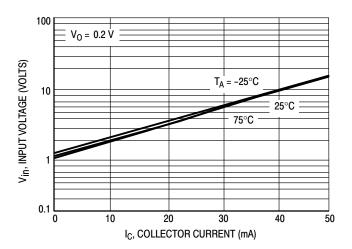


Figure 16. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS - EMC3DXV5T1 NPN TRANSISTOR

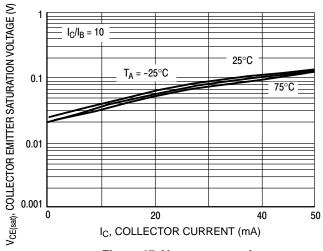


Figure 17. V_{CE(sat)} versus I_C

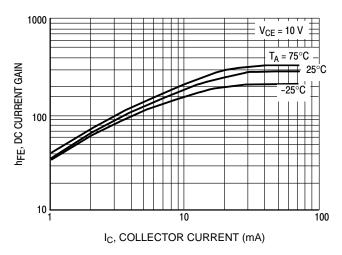


Figure 18. DC Current Gain

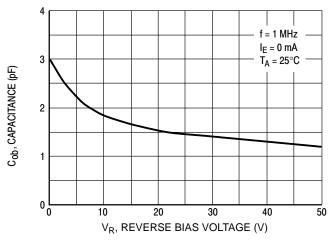


Figure 19. Output Capacitance

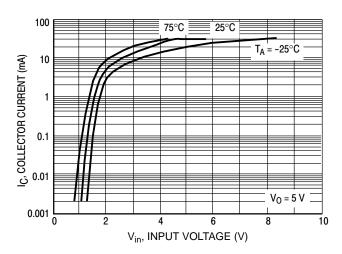


Figure 20. Output Current versus Input Voltage

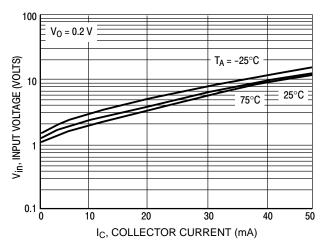


Figure 21. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS -EMC4DXV5T1 PNP TRANSISTOR

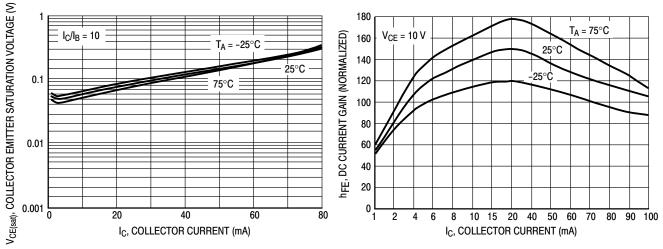


Figure 22. V_{CE(sat)} versus I_C

Figure 23. DC Current Gain

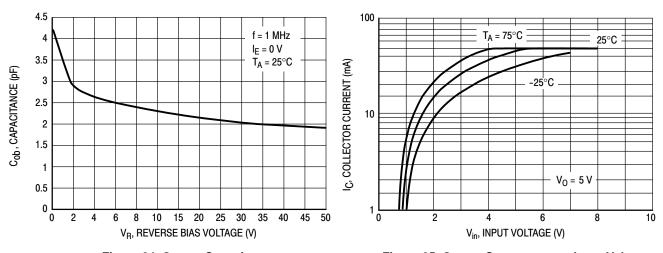


Figure 24. Output Capacitance

Figure 25. Output Current versus Input Voltage

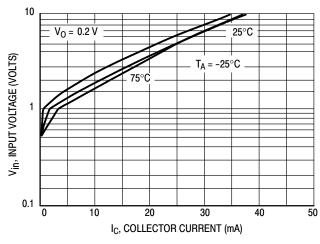


Figure 26. Input Voltage versus Output Current

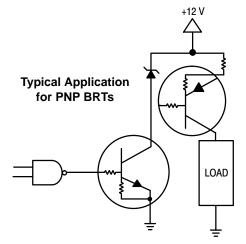


Figure 27. Inexpensive, Unregulated Current Source

TYPICAL ELECTRICAL CHARACTERISTICS - EMC5DXV5T1 PNP TRANSISTOR

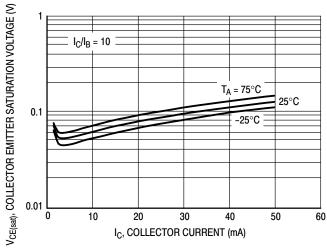


Figure 28. V_{CE(sat)} versus I_C

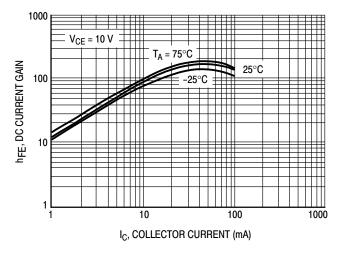


Figure 29. DC Current Gain

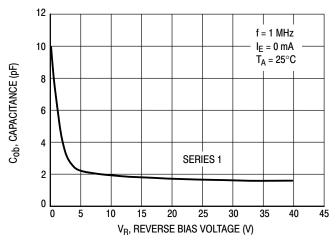


Figure 30. Output Capacitance

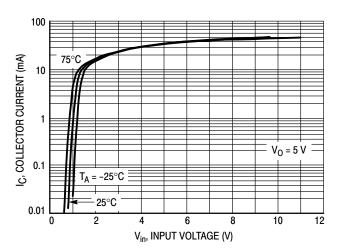


Figure 31. Output Current versus Input Voltage

TYPICAL ELECTRICAL CHARACTERISTICS - EMC4DXV5T1, EMC5DXV5T1 NPN TRANSISTOR

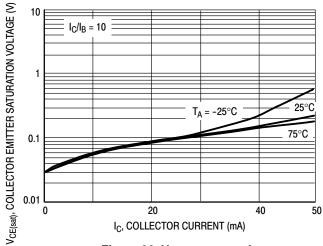


Figure 32. V_{CE(sat)} versus I_C

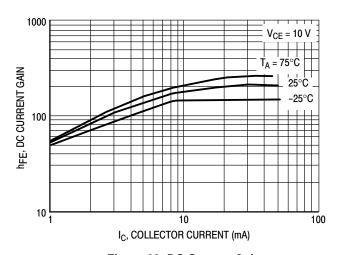


Figure 33. DC Current Gain

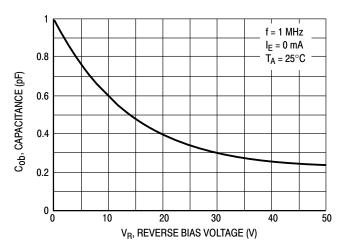


Figure 34. Output Capacitance

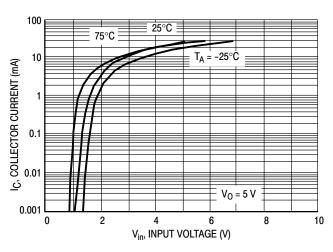


Figure 35. Output Current versus Input Voltage

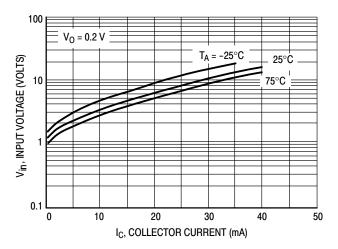
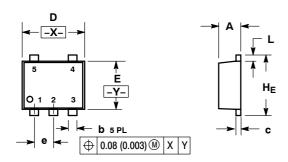


Figure 36. Input Voltage versus Output Current

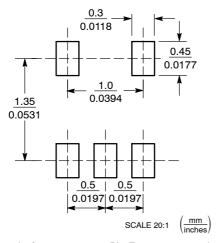


SOT-553, 5 LEAD CASE 463B ISSUE C

DATE 20 MAR 2013



RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETERS

 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH
 THICKNESS: MINIMUM LEAD THICKNESS IS THE MINIMUM
 THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
С	0.08	0.13	0.18	0.003	0.005	0.007
D	1.55	1.60	1.65	0.061	0.063	0.065
E	1.15	1.20	1.25	0.045	0.047	0.049
е		0.50 BSC		0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
He	1.55	1.60	1.65	0.061	0.063	0.065

GENERIC MARKING DIAGRAM*



XX = Specific Device Code

M = Date Code

= Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

STYLE 1: PIN 1. BASE 2. EMITTER 3. BASE 4. COLLECTOR 5. COLLECTOR	STYLE 2: PIN 1. CATHODE 2. COMMON ANODE 3. CATHODE 2 4. CATHODE 3 5. CATHODE 4	STYLE 3: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. CATHODE 1	STYLE 4: PIN 1. SOURCE 1 2. DRAIN 1/2 3. SOURCE 1 4. GATE 1 5. GATE 2	STYLE 5: PIN 1. ANODE 2. EMITTER 3. BASE 4. COLLECTOR 5. CATHODE
STYLE 6: PIN 1. EMITTER 2 2. BASE 2 3. EMITTER 1 4. COLLECTOR 1 5. COLLECTOR 2/BASE 1	STYLE 7: PIN 1. BASE 2. EMITTER 3. BASE 4. COLLECTOR 5. COLLECTOR	STYLE 8: PIN 1. CATHODE 2. COLLECTOR 3. N/C 4. BASE 5. EMITTER	STYLE 9: PIN 1. ANODE 2. CATHODE 3. ANODE 4. ANODE 5. ANODE	

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PAGE 2 OF 2

ISSUE	REVISION	DATE
Α	ADDED STYLES 3-9. REQ. BY D. BARLOW	11 NOV 2003
В	ADDED NOMINAL VALUES AND UPDATED GENERIC MARKING DIAGRAM. REQ. BY HONG XIAO	27 MAY 2005
С	UPDATED DIMENSIONS D, E, AND HE. REQ. BY J. LETTERMAN.	20 MAR 2013

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Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative